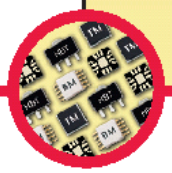
GaAs MMIC Power Amplifier



DESCRIPTION

AMCOM's AM002535MM-BM/EM/FM-R is part of the GaAs MMIC power amplifier series. It has 24 dB gain, 34 dBm output power over most of the 0.03 to 2.5 GHz band. This MMIC is in a ceramic package with both RF and DC leads at the bottom level of the package to facilitate low-cost SMT assembly to the PC board. AM002535MM-FM-R is AM002535MM-BM-R assembled on a copper flange carrier for screwing on to a metal heat sink. The EM package has the same footprint as the FM package with straight leads and a Copper/Tungsten flange instead of the Copper flange. This MMIC is RoHS compliant.

FEATURES

- Wide bandwidth from 0.03 to 2.5 GHz
- High output power, P1dB = 34 dBm
- High gain, 24dB
- Input & output 50-ohm impedance

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE*

(V_{dd} = +20V, I_{dd1} = 150mA, I_{dd2} = 400mA, V_{gs1} = -0.9V**, I_{gg1}<1mA, V_{gs2} = -0.9V**, I_{gg2}<2mA, T_a = 25°C)

Parameters	Minimum	Typical	Maximum
Frequency	0.1 – 2.0GHz	0.03 – 2.5GHz	-
Small Signal Gain	20 dB	24 dB	28 dB
Gain Ripple	-	± 1.0 dB	± 2.0 dB
P_{1dB} (0.1 to 2GHz)	32.5 dBm	34 dBm	-
P_{sat} (0.1 to 2GHz)	33.5 dBm	35 dBm	-
Efficiency @ P_{sat}	-	25 %	
IP3 @ 1GHz	-	45 dBm	
Input Return Loss	10 dB	15dB	
Output Return Loss	6 dB	8dB	
Thermal Resistance		8 °C/W	

*Specifications subject to change without notice. ** V_{gs1} & V_{gs2} may vary from lot to lot.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating
Drain source voltage	V_{dd}	24 V
Gate source voltage	V_{gg1} , V_{gg2}	-5 V
Drain source current	I_{dd1} +I_{dd2}	0.8 A
Continuous dissipation at room temperature	P_t	18 W
Channel temperature	T_{ch}	175 °C
Storage temperature	T_{sto}	-55°C to +135°C

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SMALL SIGNAL DATA*

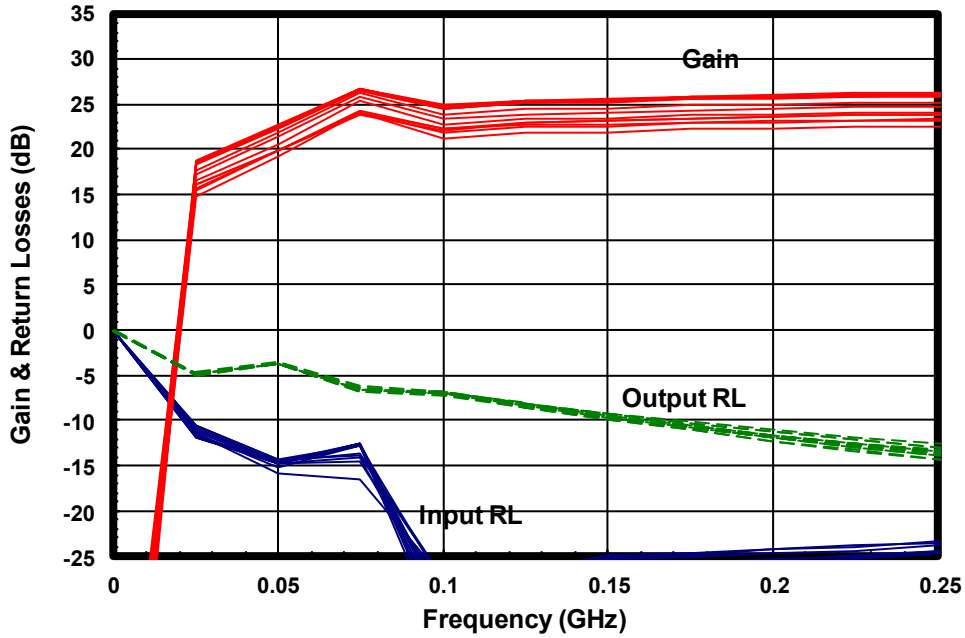


Figure 1: Gain and input/output return loss at low frequency

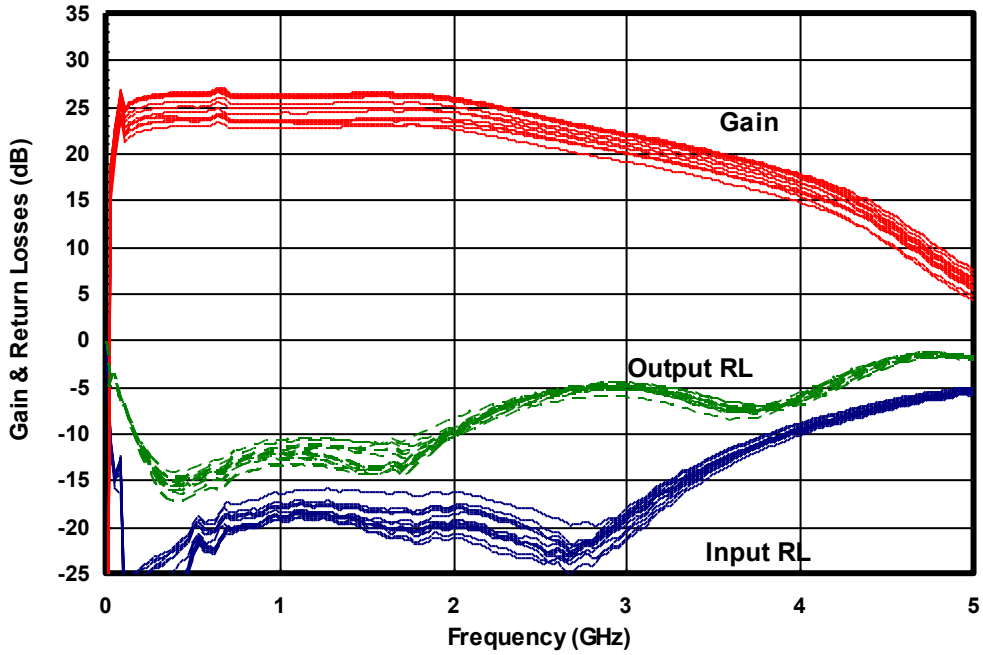


Figure 2: Gain and input/output return loss at RF & microwave frequencies

*Measurements performed with bias tee on multiple MMICs. (Bias: V_{dd1} = V_{dd2} = 20V, I_{dd1} = 0.15A, I_{dd2} = 0.4A)

POWER DATA*

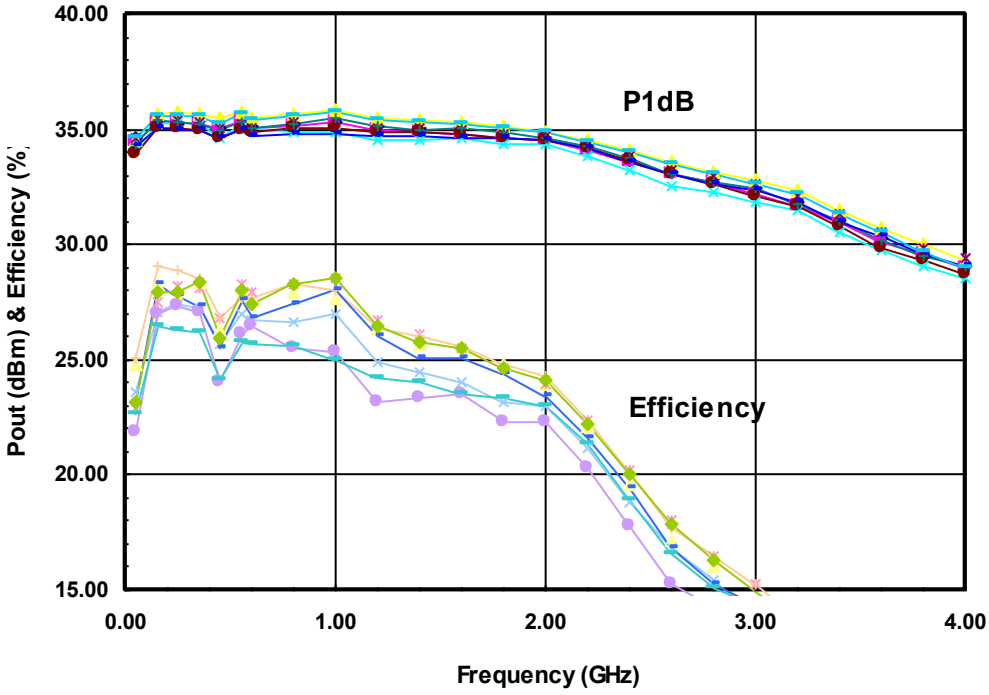


Figure3: P_{1dB} and efficiency versus frequency

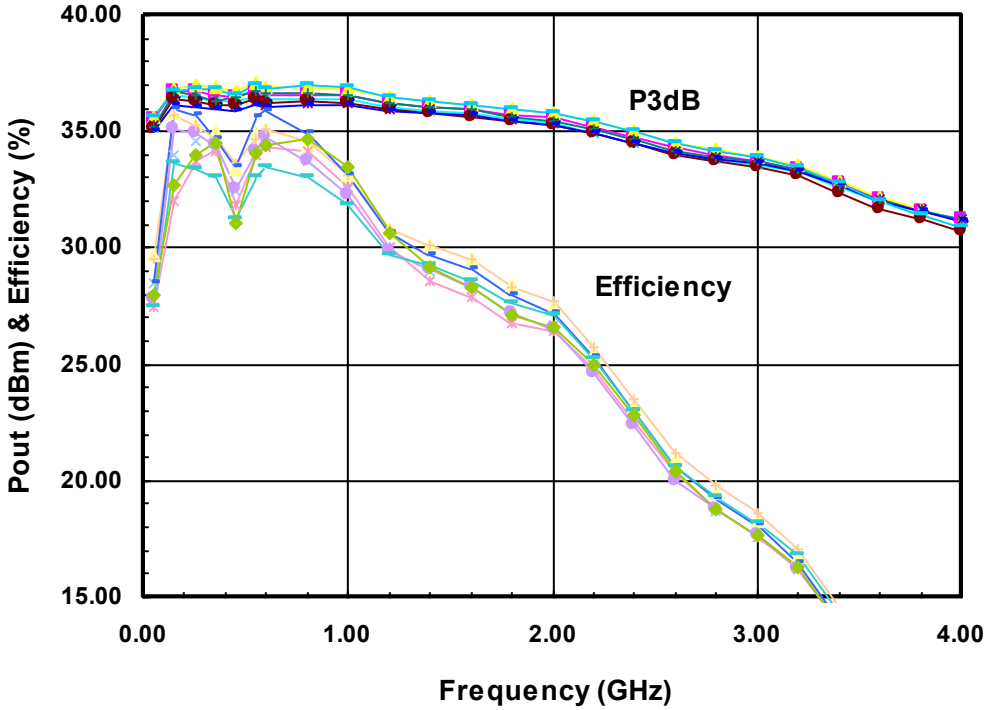


Figure4: P_{3dB} and efficiency versus frequency

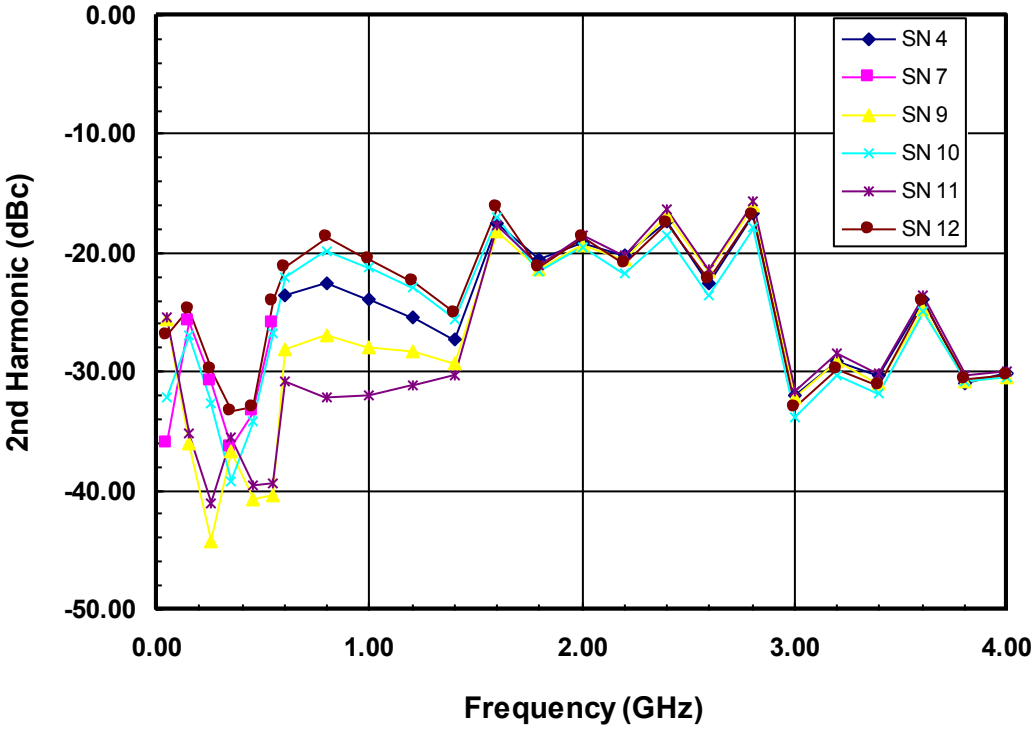


Figure 5: Second harmonic at P_{1dB} versus frequency

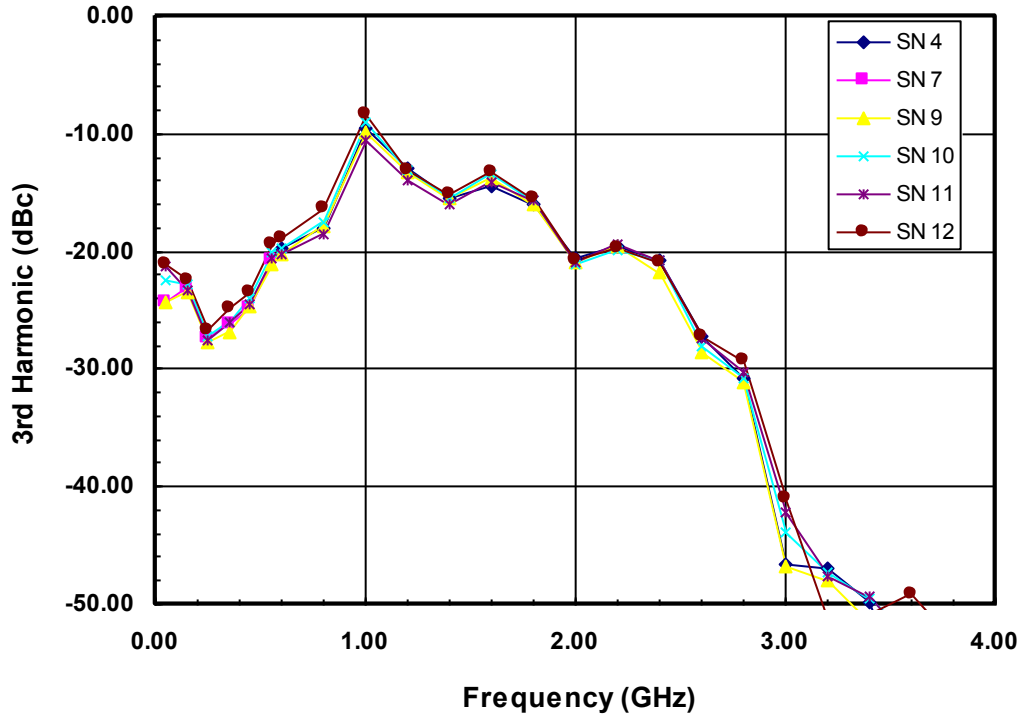


Figure 6: Third harmonic at P_{1dB} versus frequency

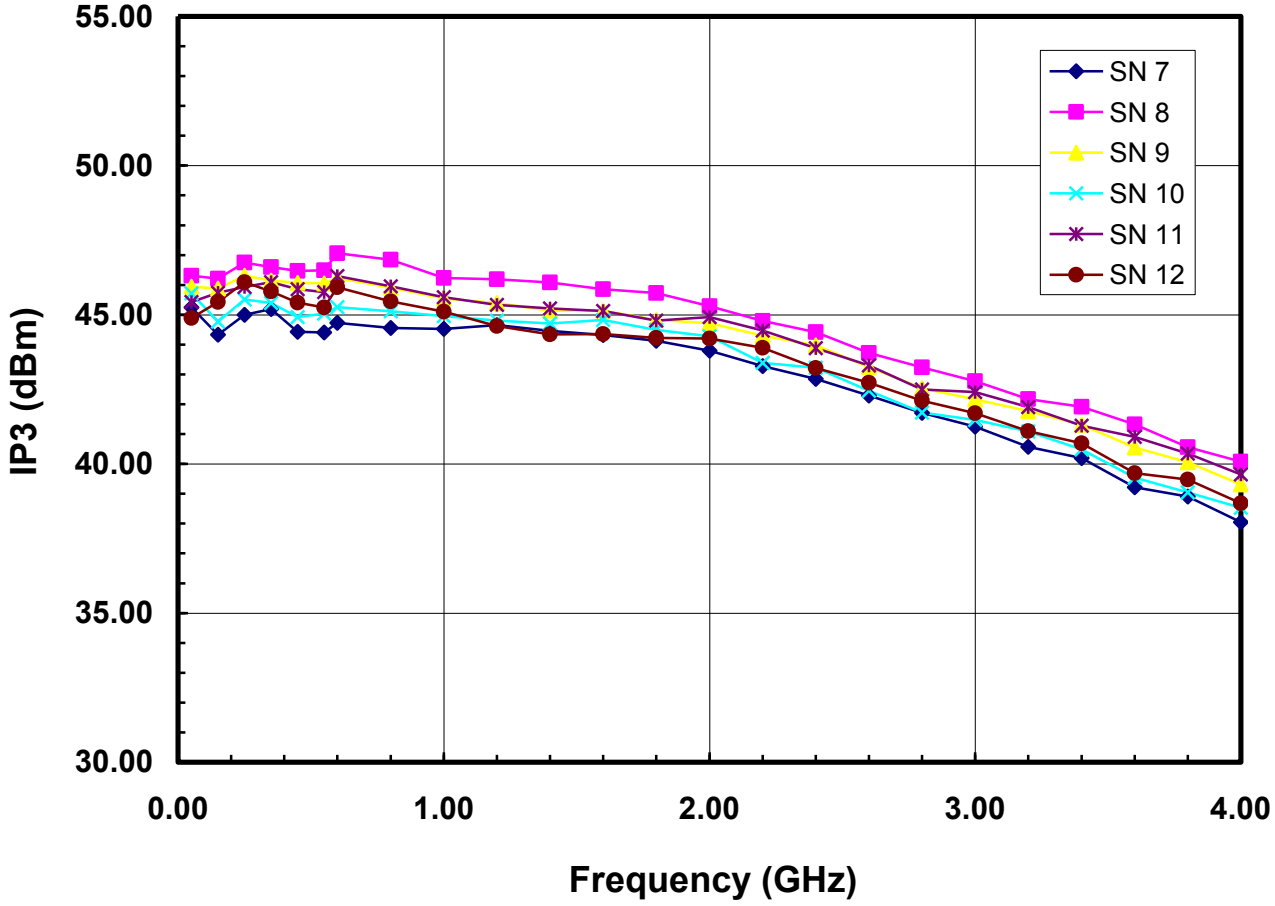
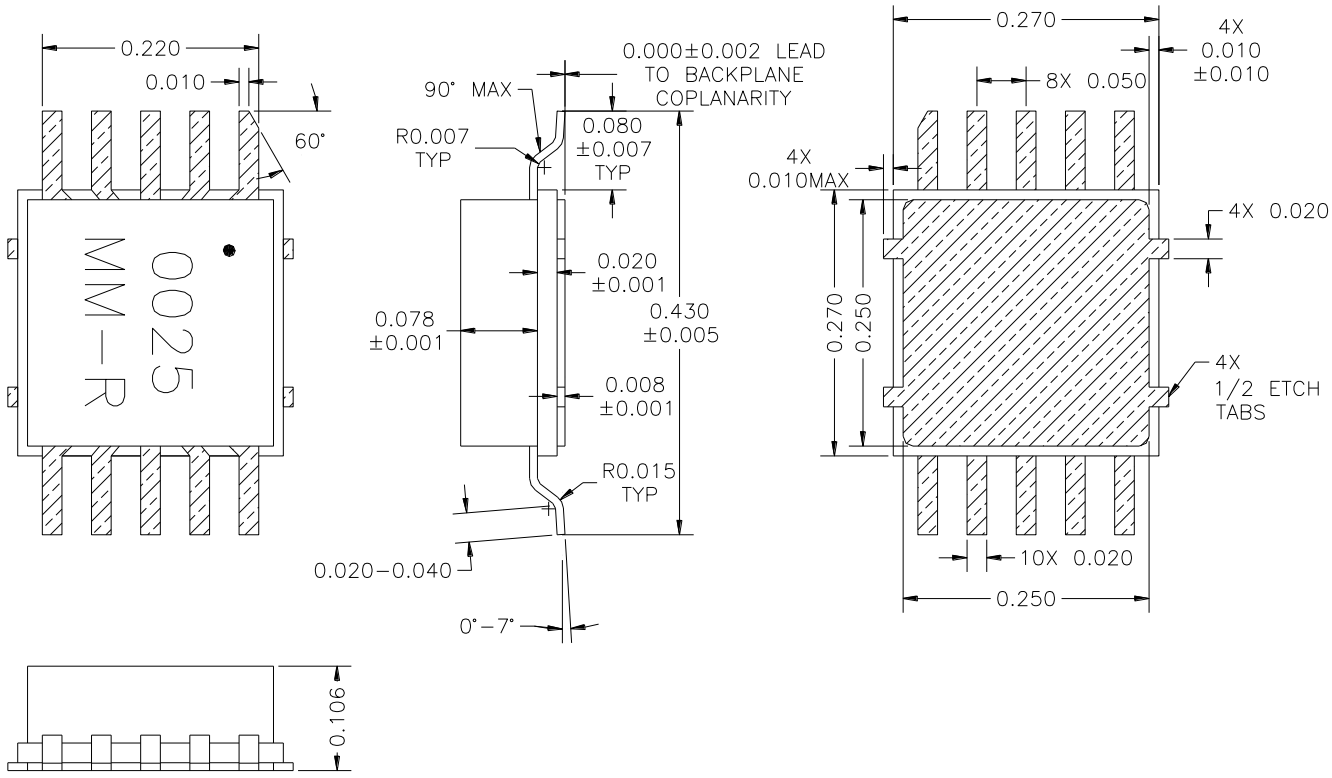


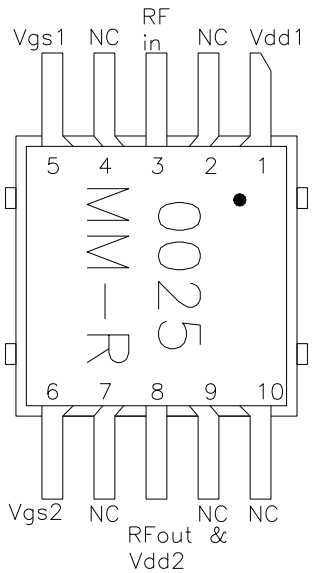
Figure 7: Third order intercept point versus frequency

*Measurements performed with bias tee on multiple MMICs. (Bias: V_{dd1} = V_{dd2} = 20V, I_{dd1}=0.15A, I_{dd2}=0.4A)

PACKAGE OUTLINE (BM)



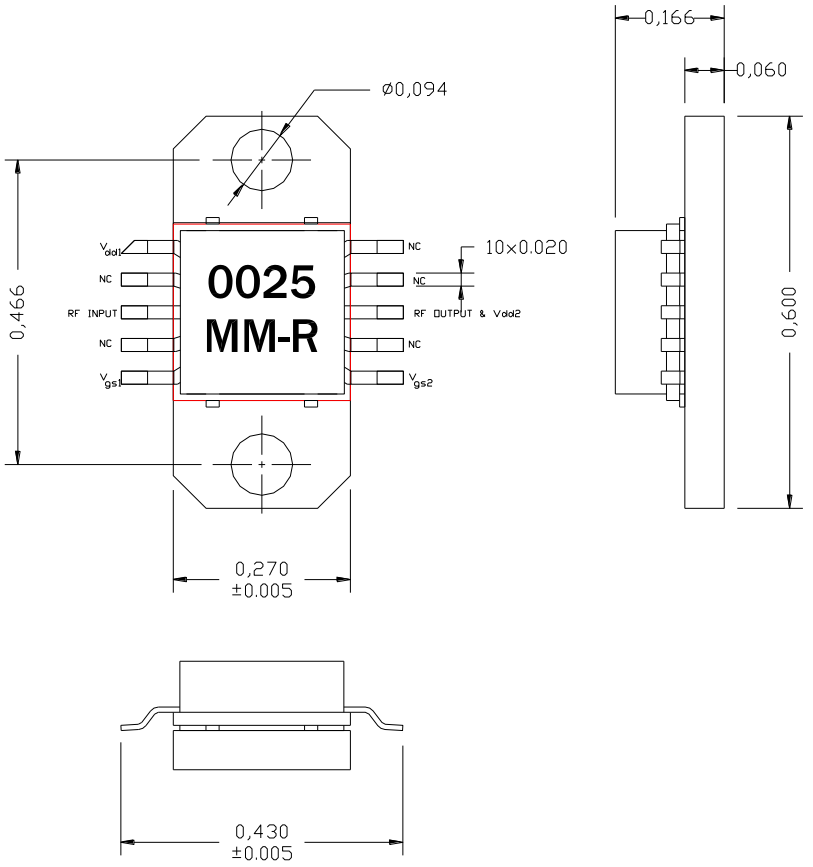
PIN LAYOUT



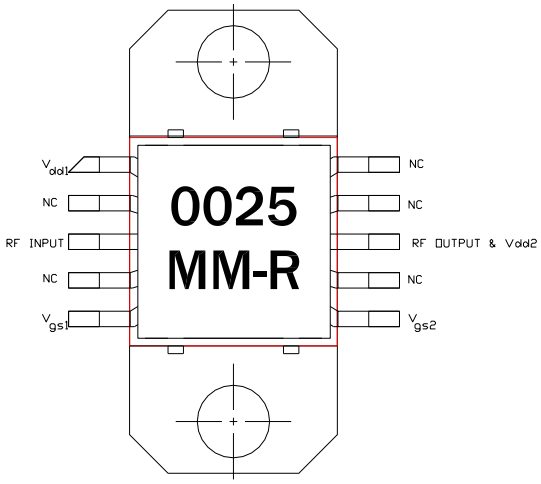
Pin No.	Function	Bias**
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-0.9V
6	Vgs2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

** V_{gs1} & V_{gs2} may vary from lot to lot

PACKAGE OUTLINE (FM)*



PIN LAYOUT

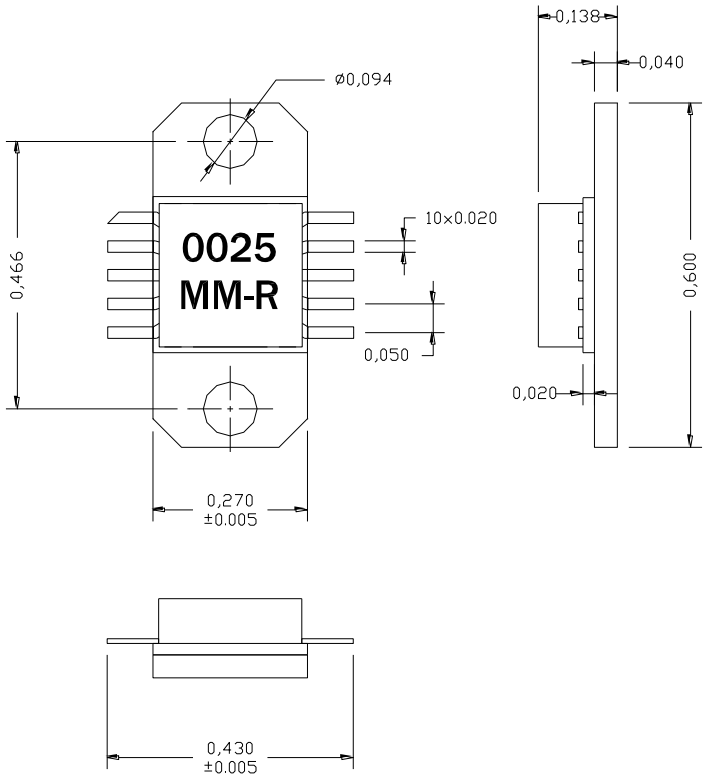


Pin No.	Function	Bias**
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-0.9V
6	Vgs2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

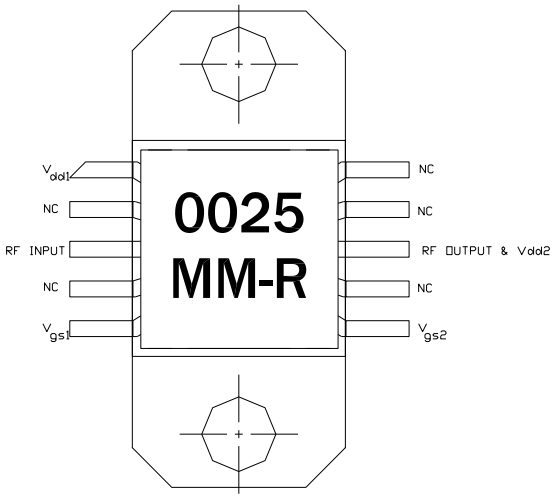
* FM version flange is made of Copper

** V_{gs1} & V_{gs2} may vary from lot to lot

PACKAGE OUTLINE (EM)*



PIN LAYOUT

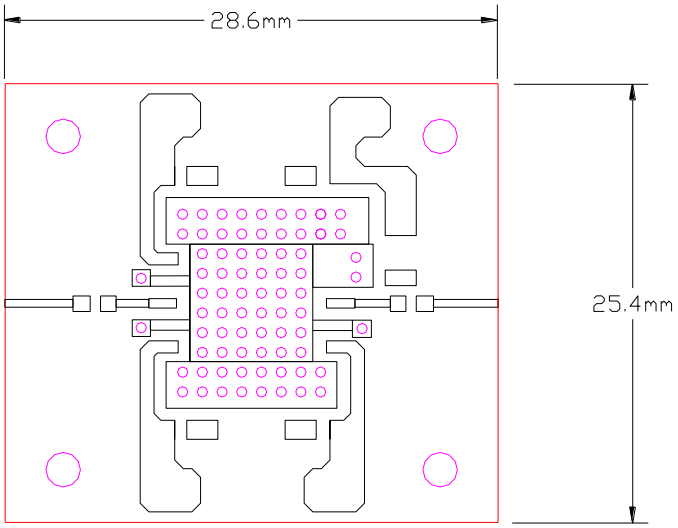


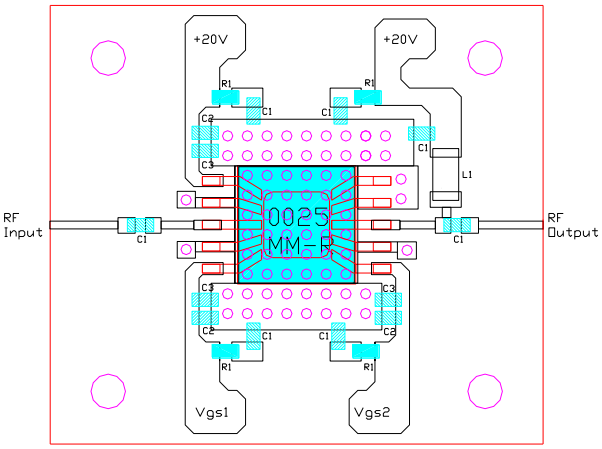
Pin No.	Function	Bias**
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-0.9V
6	Vgs2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* EM version flange is made of CuW

** V_{gs1} & V_{gs2} may vary from lot to lot

TEST CIRCUIT (BM Package)





Notes:
1- Material is 10mils FR4 with 1 Oz Copper
2- All vias are plated thru
MIN. via metal thickness = 25um
3- R1=500hms, R2=00hms,
C1=1000pF, C2=100pF, C3=20pF, L1=300nH
4- Bias could be supplied to the RF output port using a bias tee.

Important Notes:

1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).

2- Recommended current biases are 150mA and 400mA for the first stage and second stage respectively. At V_{dd1} & V_{dd2} = +20V V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively. V_{gs1} & V_{gs2} values could vary from lot to lot.

3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2}.

4- The current flowing out of the V_{gs1} & V_{gs2} pin is less than 100 & 200µA respectively at low power. At P1dB the currents could go up to 1mA and 2mA respectively at P_{1dB}.