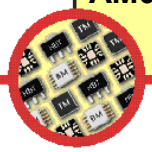
GaAs MMIC Power Amplifier



AM008030WM-BM-R
AM008030WM-EM-R
AM008030WM-FM-R
October 2018
Rev 6

DESCRIPTION

AMCOM's AM008030WM-BM/EM/FM-R is an ultra-broadband GaAs MMIC power amplifier. It has 18dB gain, and >28dBm output power over the 0.05 to 10GHz band. This MMIC is in a ceramic package with both RF and DC leads at the bottom level of the package to facilitate low-cost SMT assembly to the PC board. AM008030WM-FM-R is AM008030WM-BM-R assembled on a gold-plated Copper flange carrier for screwing on to a metal heat sink. AM008030WM-EM-R is identical to AM008030WM-FM-R with a CuW flange instead of Copper and straight leads. All 3 components are RoHS compliant.

FEATURES

- Ultra wide bandwidth from 50MHz to 10GHz
- High output power, P1dB = 30.5dBm
- High gain, 18dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE * (Bias Conditions**: V_{dd} = +12V, I_{dq} = 400mA)

Parameters	Minimum	Typical **	Maximum
Frequency	0.1 – 8GHz	0.05 – 10GHz	
Small Signal Gain	14dB	18dB	22dB
Gain Ripple		± 3dB	± 4.0dB
P1dB @ 2GHz	29dBm	30dBm	
P1dB from 0.1 to 8GHz		> 27dBm	
Psat @ 2GHz	30dBm	31dBm	
Psat from 0.1 to 8.0GHz		> 28dBm	
IP3 @ 1GHz		48dBm	
Input Return Loss	9dB***	15dB	
Output Return Loss	7dB***	10dB	
Thermal Resistance		4.5°C/W	

* Specifications subject to change without notice.

** Gate biases corresponding to above currents are V_{gs1}=-0.7V, I_{gs1} < 0.5mA, V_{gs2}=-0.7V, I_{gs2} < 1mA and may vary from lot to lot. Gate currents could reach above limits only near power saturation. DC block needed at input & bias tee at the output.

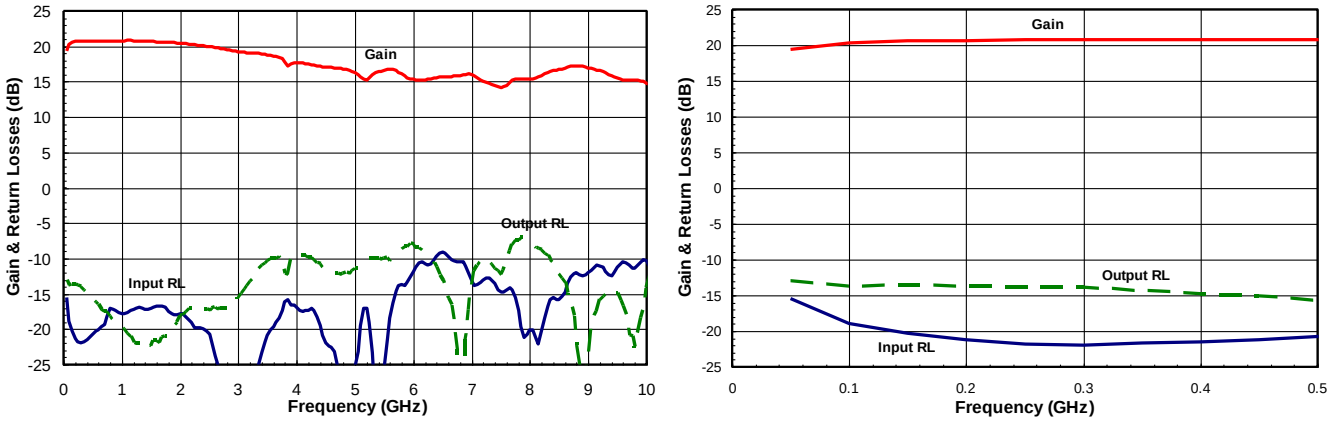
*** Minimum return loss for FM version is guaranteed up to 5GHz

Email: info@amcomusa.com
Website: www.amcomusa.com
Tel. (301) 353-8400 Fax. (301) 353-8401
401 Professional Drive, Gaithersburg, MD 20879

ABSOLUTE MAXIMUM RATING

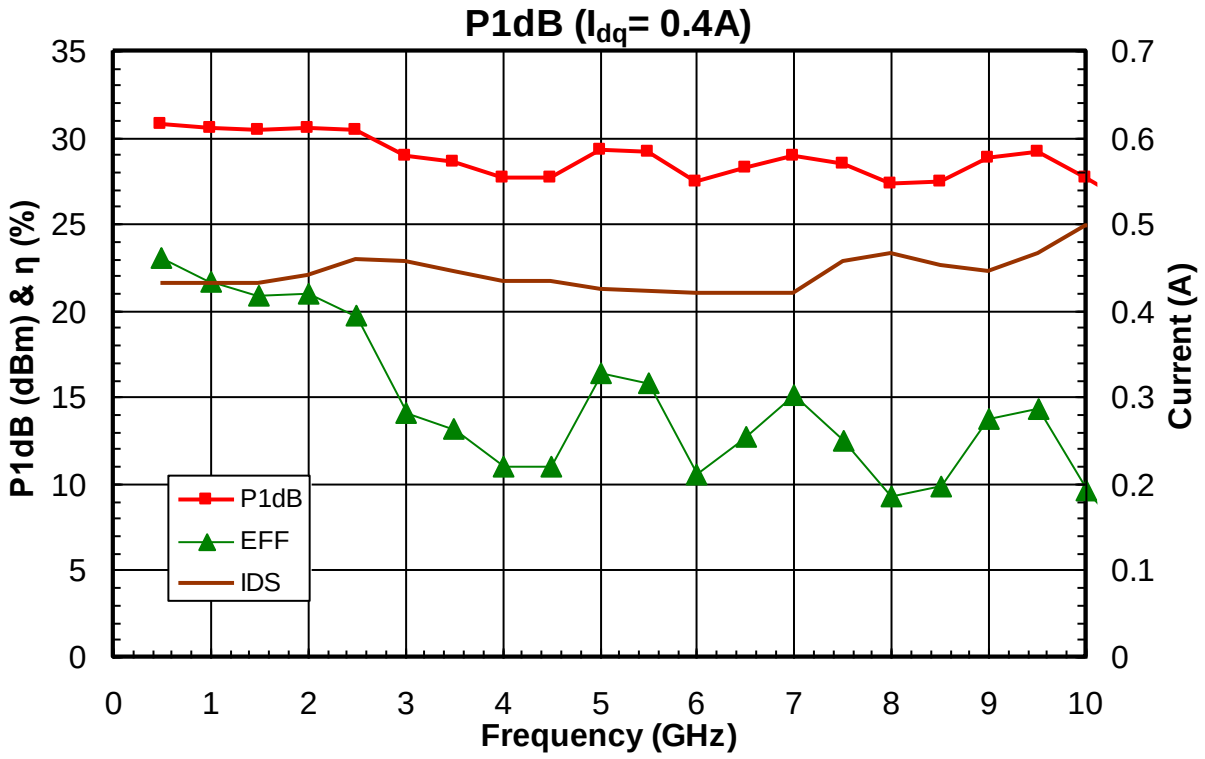
Parameters	Symbol	Rating
Drain source voltage	V_{dd}	13V
Gate source voltage	V_{gs1} & V_{gs2}	-3V
Drain source current	I_{dq1}	0.2A
Drain source current	I_{dq2}	0.40A
Continuous dissipation at 25ºC	P_t	7.8W
Channel temperature	T_{ch}	175°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

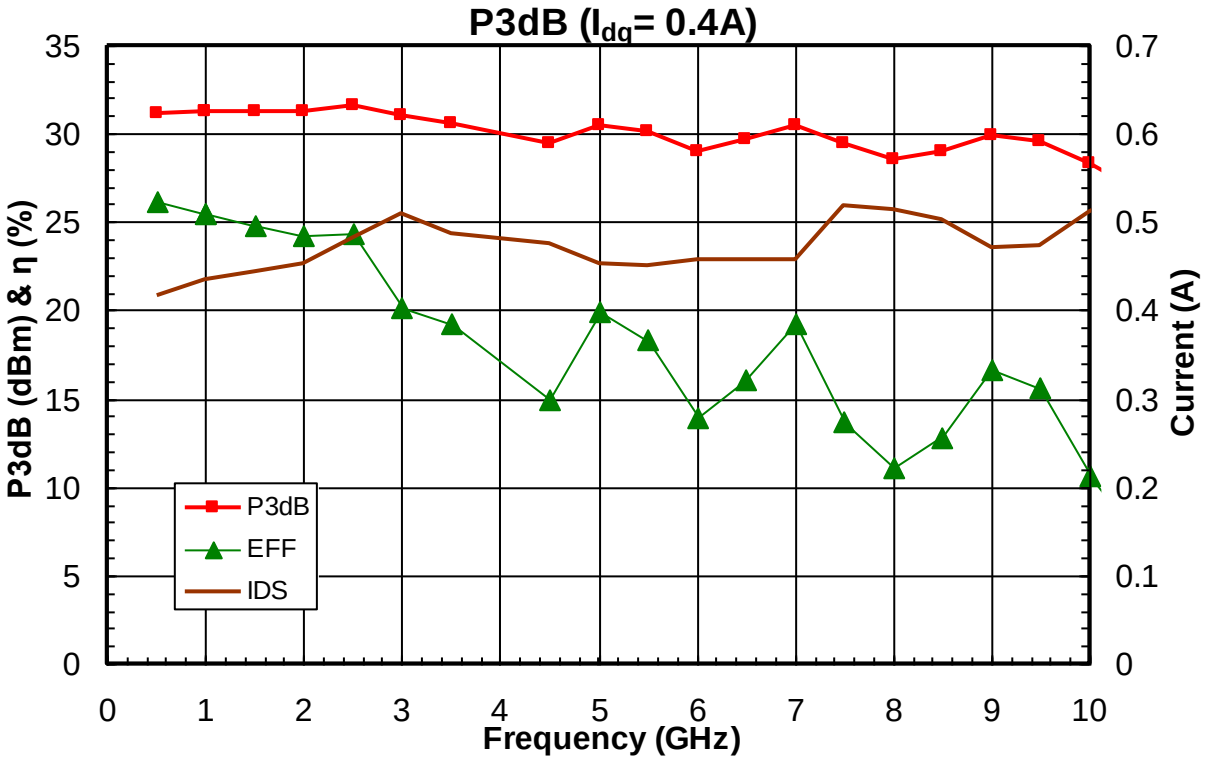
SMALL SIGNAL DATA*



* S-Parameters measured using bias tee at the output. MMIC could be operated at lower than V_{dd}=+12V with almost same small signal parameters.

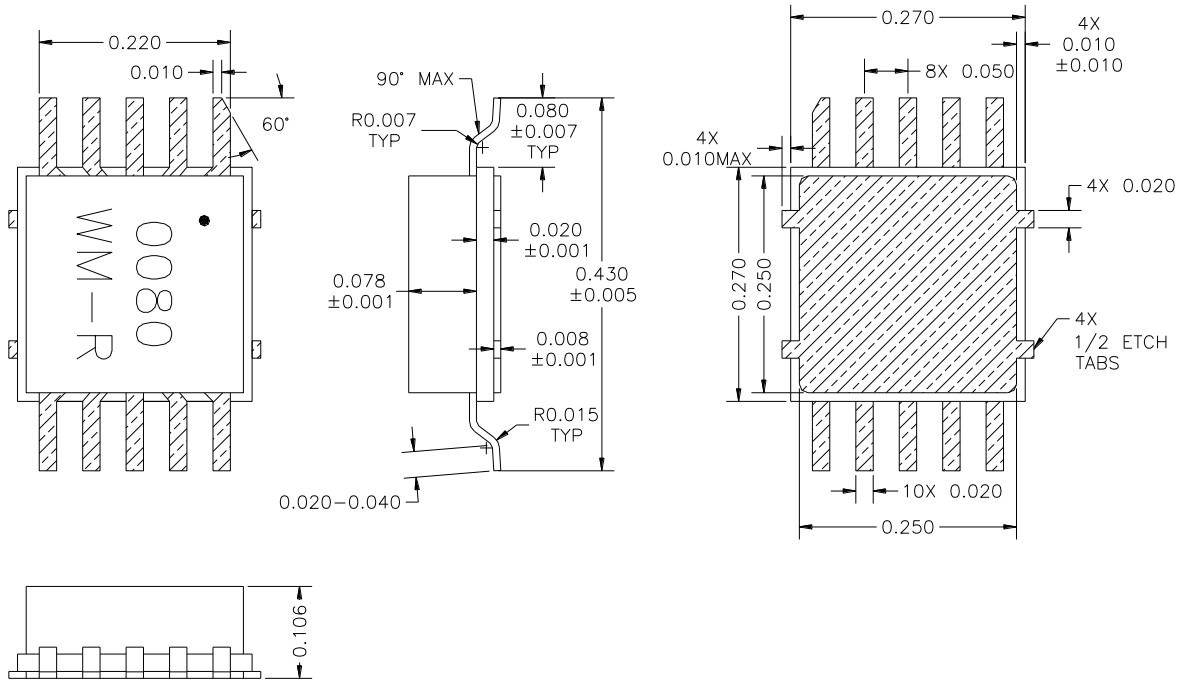
POWER DATA*





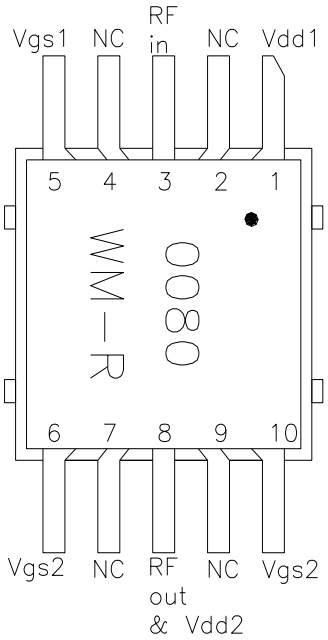
* Power measured using bias tee at the output. MMIC could be operated at lower than V_{dd}=+12V with reduced power output.

PACKAGE OUTLINE (BM)



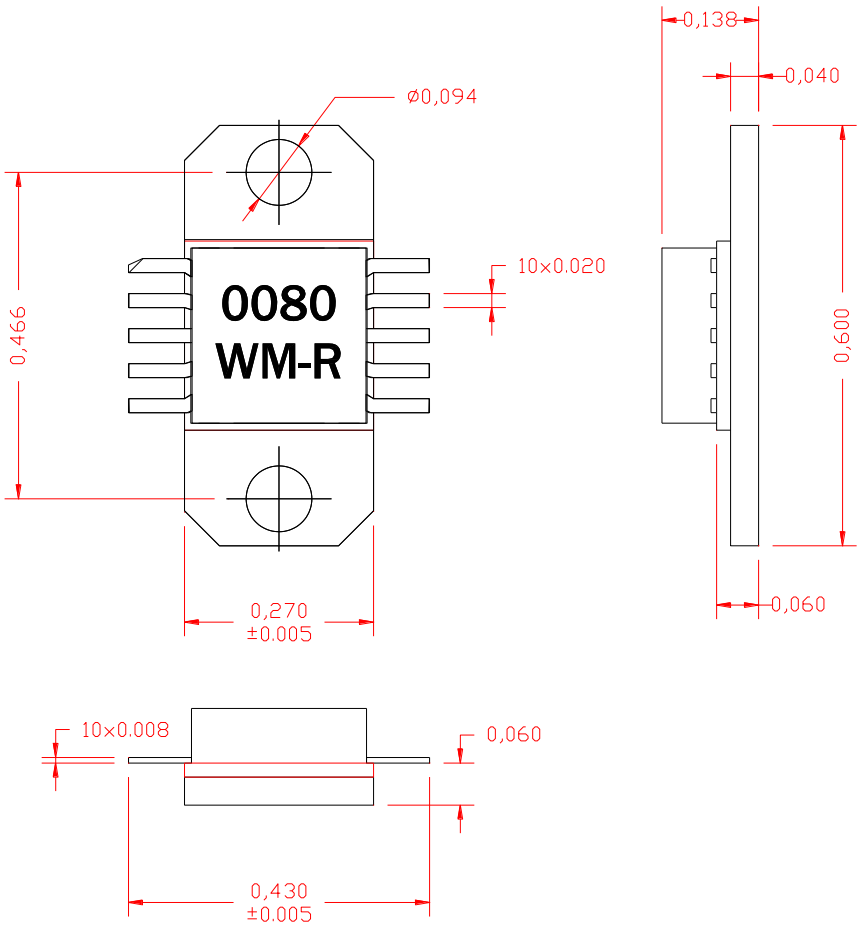
- Gate biases are for reference only and may vary from lot to lot

Pin Layout

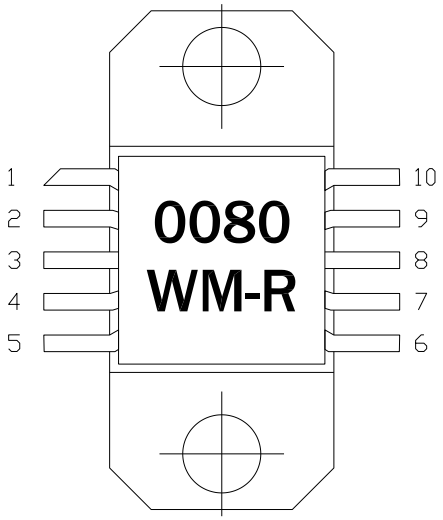


Pin No.	Function	Bias
1	Vdd1	+12V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-0.7V
6	Vgs2	-0.7V
7	NC	
8	RF out & Vdd2	+12V
9	NC	
10	Vgs2	

PACKAGE OUTLINE (EM)

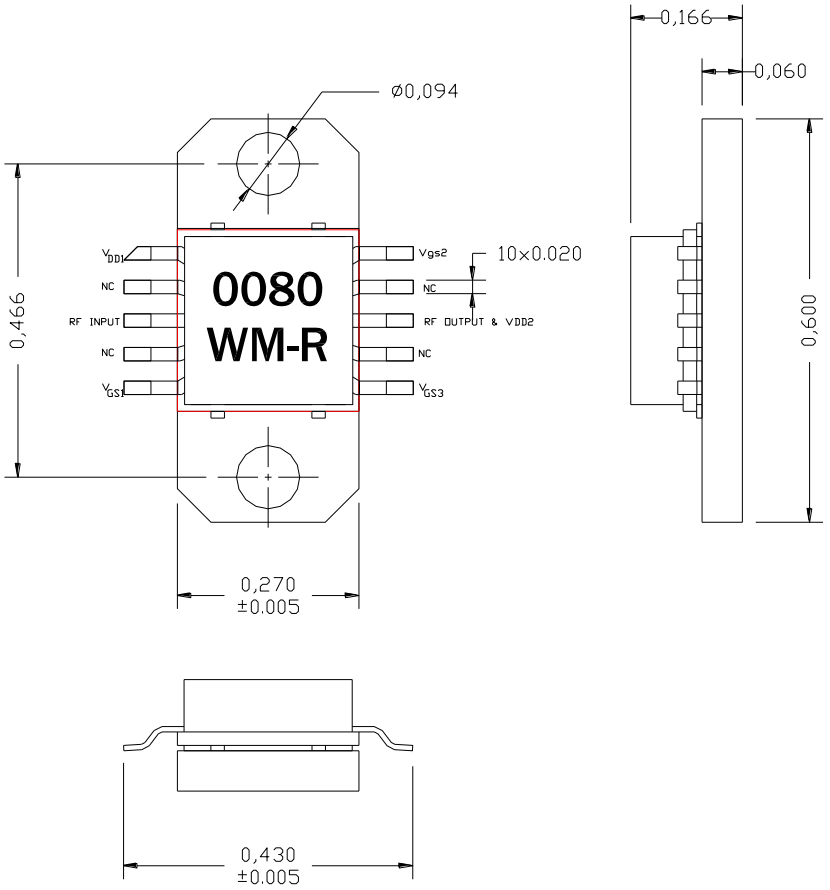


Pin Layout

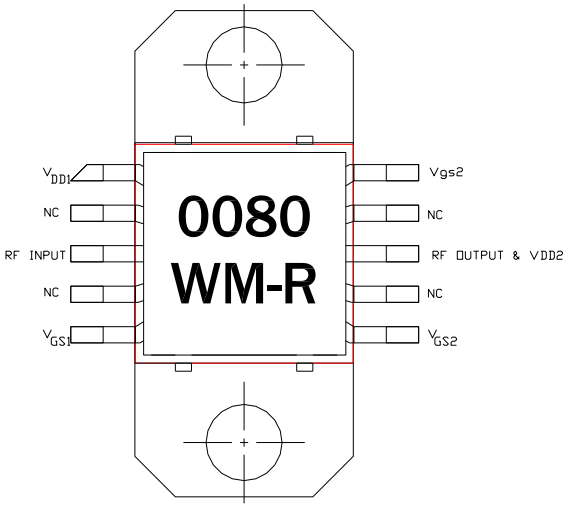


Pin No.	Function	Bias
1	Vdd1	+12V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-0.7V
6	Vgs2	-0.7V
7	NC	
8	RF out & Vdd2	+12V
9	NC	
10	Vgs2	

PACKAGE OUTLINE (FM)

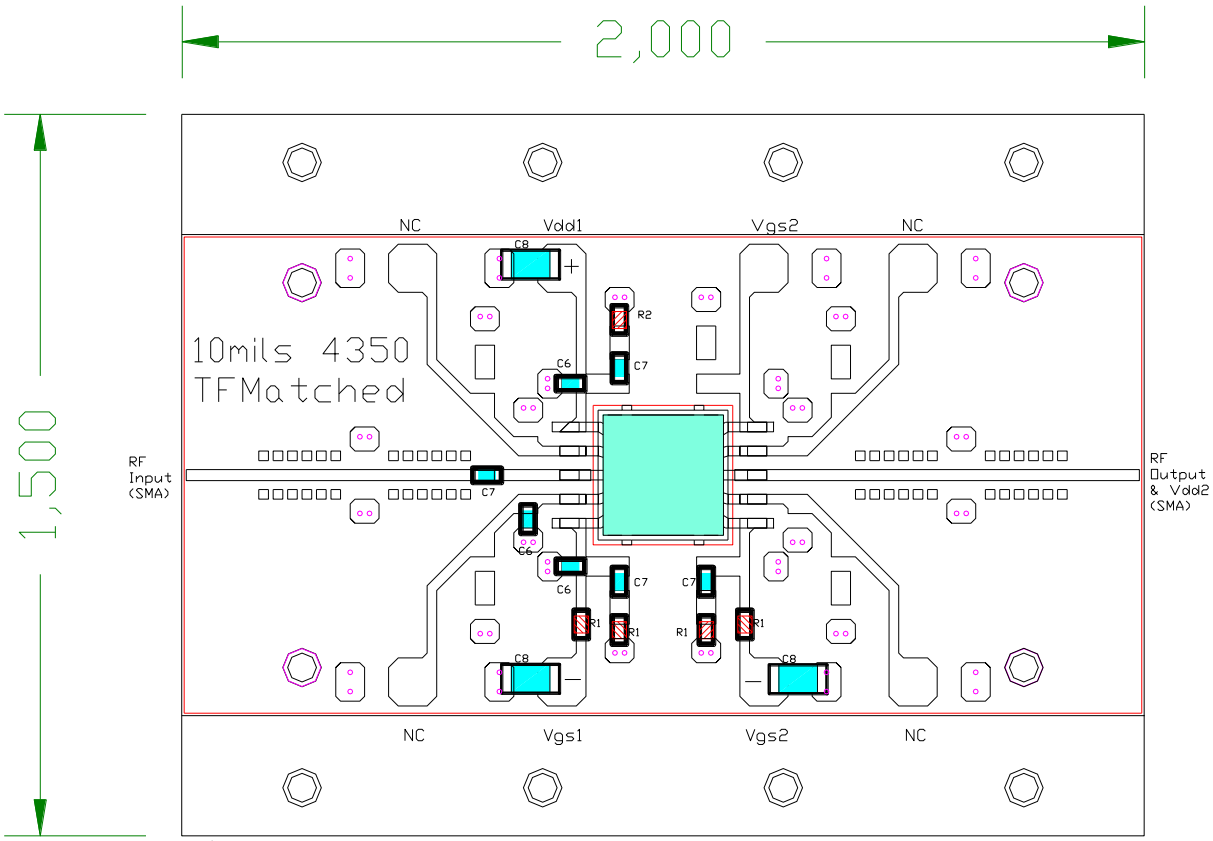


Pin Layout



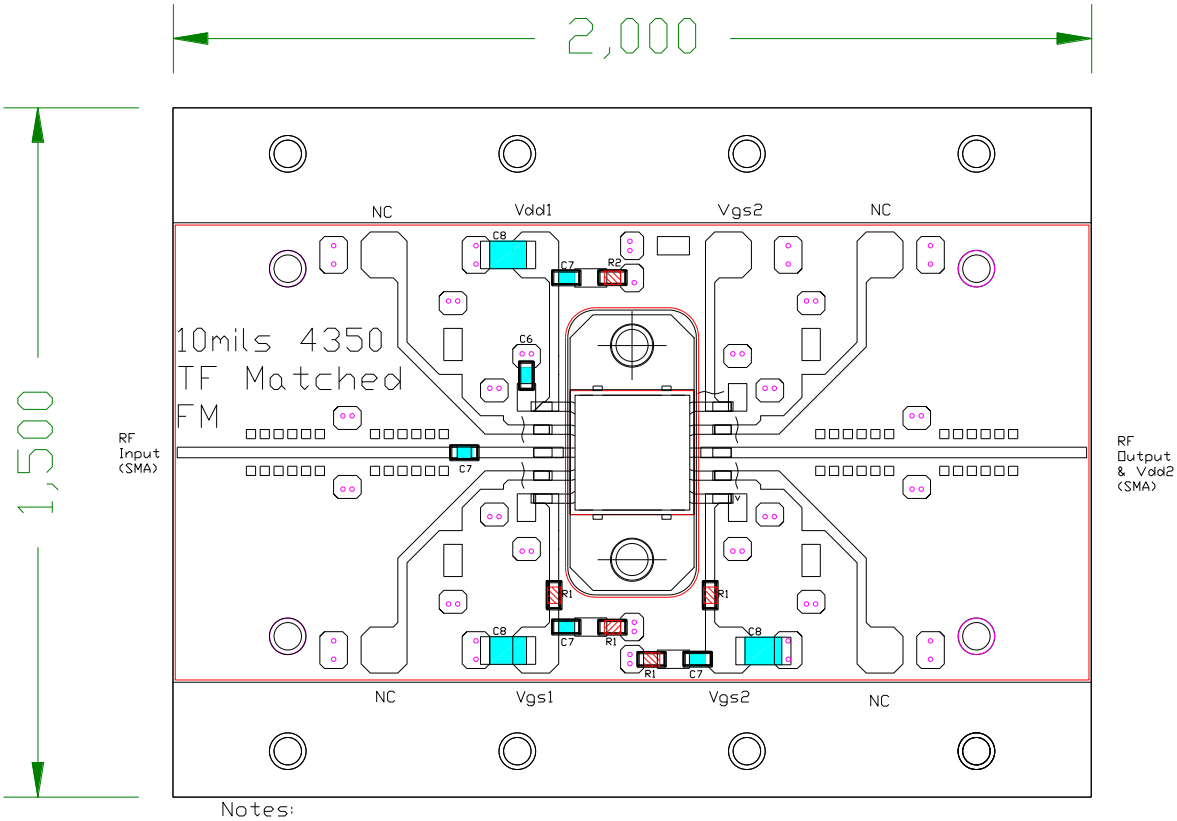
Pin No.	Function	Bias
1	Vdd1	+12V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-0.7V
6	Vgs2	-0.7V
7	NC	
8	RF out & Vdd2	+12V
9	NC	
10	Vgs2	

TEST CIRCUIT for BM Package



Notes:
1- 10mils Rogers 4350 Material epoxied
2- Ckt is for matched MMICs
3- C6=20pf, C7=1000pF, C8=10uF
   R1=50 Ohms, R2=10 Ohms, R3=5 Ohms
4- All Caps & Resistors are 0603 size except for C8: 1206 size
5- Bias tee should be used at output.

TEST CIRCUIT for FM & EM Packages



Notes:
1- 10mils Rogers 4350 Material epoxied
2- Ckt is for matched MMICs
3- C6=20pf, C7=1000pF, C8=10uF
   R1=50 Ohms, R2=10 Ohms, R3=5 Ohms
4- All Caps & Resistors are 0603 size except for C8: 1206 size
5- Bias tee should be used at output.
6- Unused bias lines should be cut to avoid ripples and resonances
7- Fixture used for both FM & EM packages

Important Notes:

1- The +12V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).

2- Recommended current biases are 130mA and 270mA for the first stage and second stage respectively. Gate biases of -0.7V are for reference only. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively.

3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2}.

4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 0.5mA & 1mA respectively at P_{1dB}.

5- External 1 µF dipped tantalum capacitor should be attached to V_{dd1} and $V_{gs1,2}$ to decouple external bias leads.

6- DC block needed at input & bias tee at the output.