

DESCRIPTION

AMCOM's AM009024WM-QN5-R is an ultra-broadband GaAs MMIC power amplifier. It has 22dB gain, and 24dBm output power over the 0.05 to 9GHz band. This MMIC is in a QFN package with both RF and DC leads at the bottom level of the package to facilitate low-cost SMT assembly to the PC board. The ground pad should have a good heat sink to dissipate the DC power. This MMIC is RoHS compliant.

FEATURES

- Ultra wide bandwidth from 50MHz to 9GHz
- Driver power = 24dBm
- High gain, 22dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE * (Bias Conditions**: $V_{dd} = +12V$, $I_{dq} = 250mA$)

Parameters	Minimum	Typical **	Maximum
Frequency	0.1 – 8GHz	0.05 – 9GHz	
Small Signal Gain	18dB	22dB	26dB
Gain Ripple		± 3dB	± 4.0dB
P1dB from 0.1 to 9GHz	22dBm	24dBm	
Psat from 0.1 to 9GHz	24dBm	25dBm	
IP3 @ 1GHz		30dBm	
Input Return Loss	4dB	7dB	
Noise Figure (0.5 to 6GHz)		6dB	7dB
Output Return Loss	7dB	10dB	
Thermal Resistance		20°C/W	

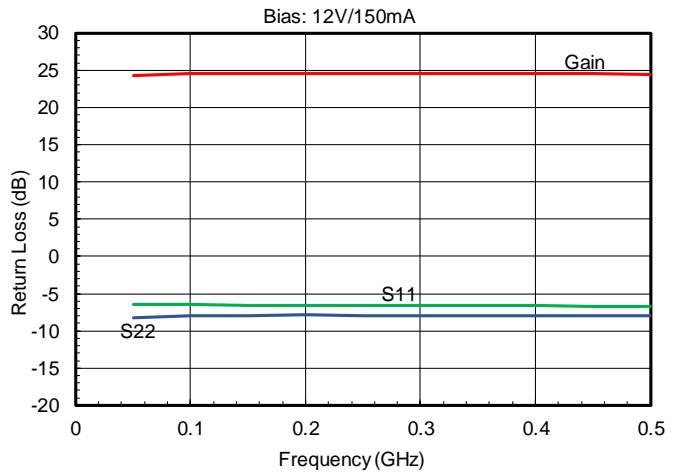
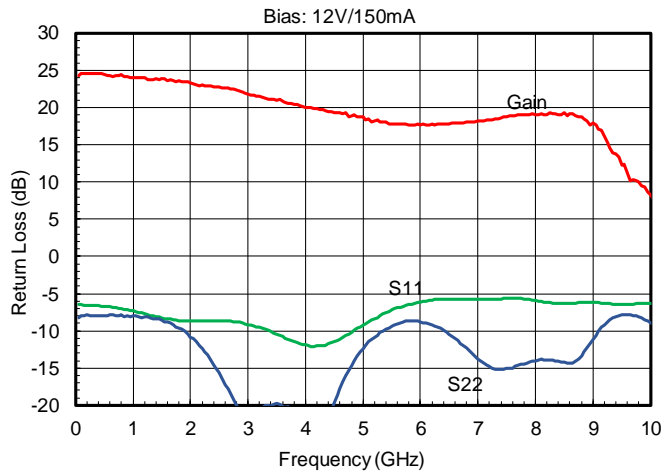
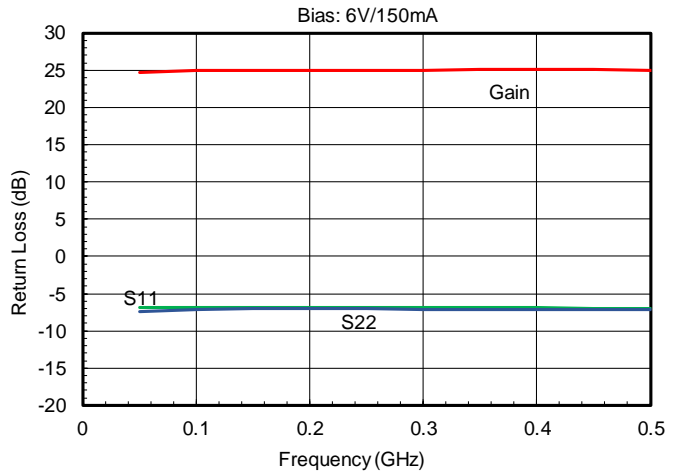
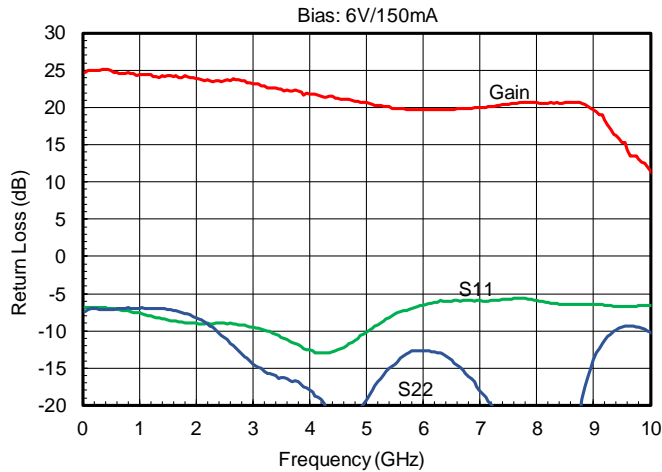
* Specifications subject to change without notice.

** Gate biases corresponding to above currents are $V_{gs1} = -0.7V$, $I_{gs1} < 0.5mA$, $V_{gs2} = -0.7V$, $I_{gs2} < 1mA$ and may vary from lot to lot. Gate currents could reach above limits only near power saturation. DC block needed at input & at the output.

ABSOLUTE MAXIMUM RATING

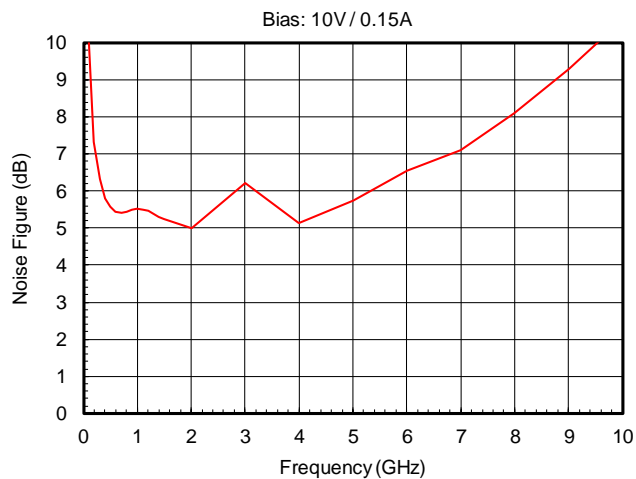
Parameters	Symbol	Rating
Drain source voltage	V _{dd}	13V
Gate source voltage	V _{gs1} & V _{gs2}	-5V
Drain source current	I _{dq1}	0.2A
Drain source current	I _{dq2}	0.3A
Continuous dissipation at 25°C	P _t	6.5W
Channel temperature	T _{ch}	175°C
Operating temperature	T _{op}	-55°C to +85°C
Storage temperature	T _{sto}	-55°C to +135°C

SMALL SIGNAL DATA*



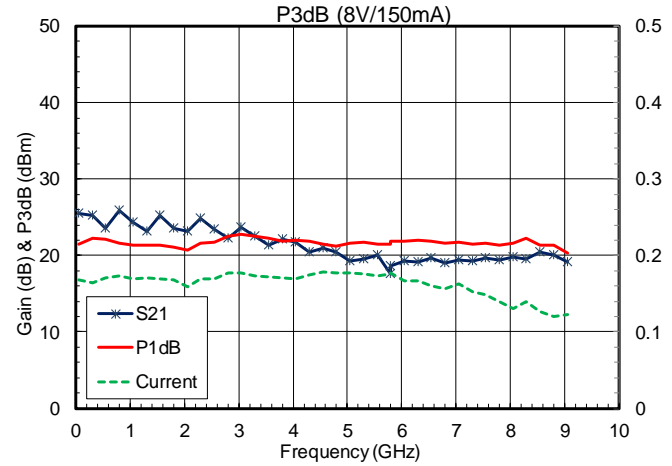
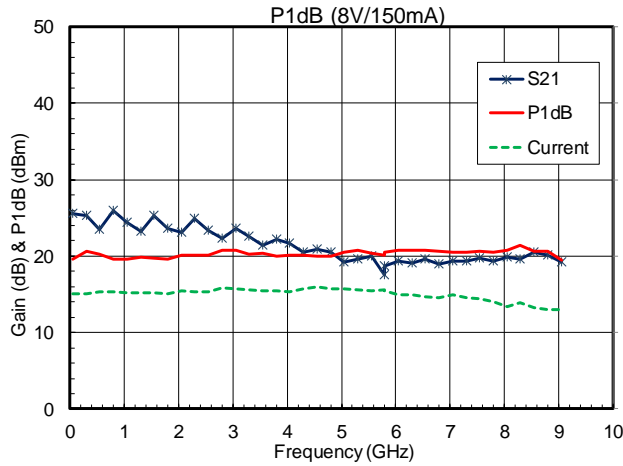
* S-Parameters measured using bias tee at the output. MMIC could be operated at lower than V_{dd}=+12V with almost same small signal parameters.

NOISE FIGURE

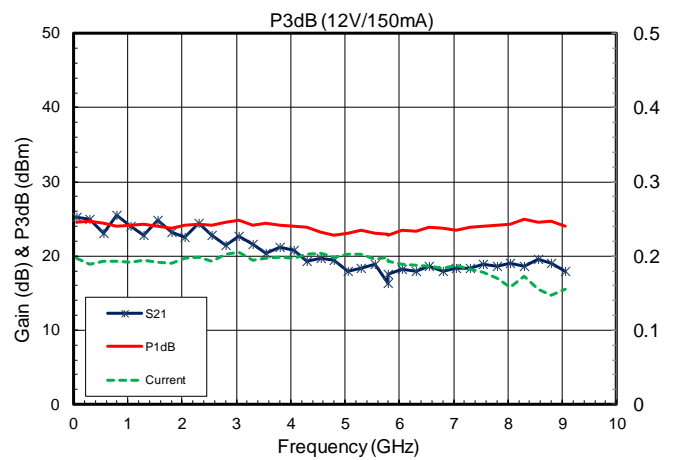
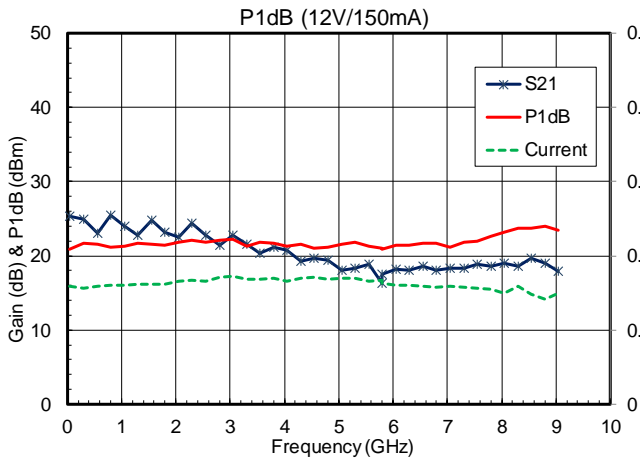


POWER DATA*

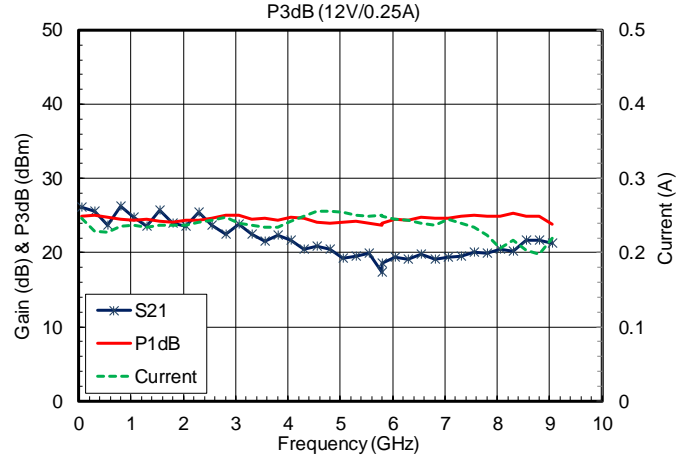
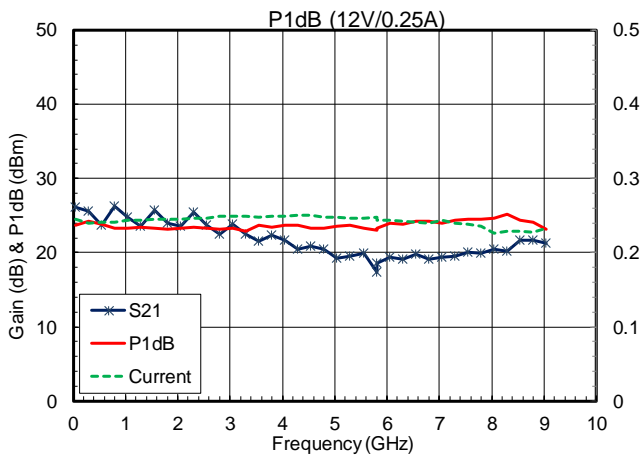
A) Power at $V_{dd} = +8V$ & $I_{dq} = 150mA$



B) Power at $V_{dd} = +12V$ & $I_{dq} = 150mA$

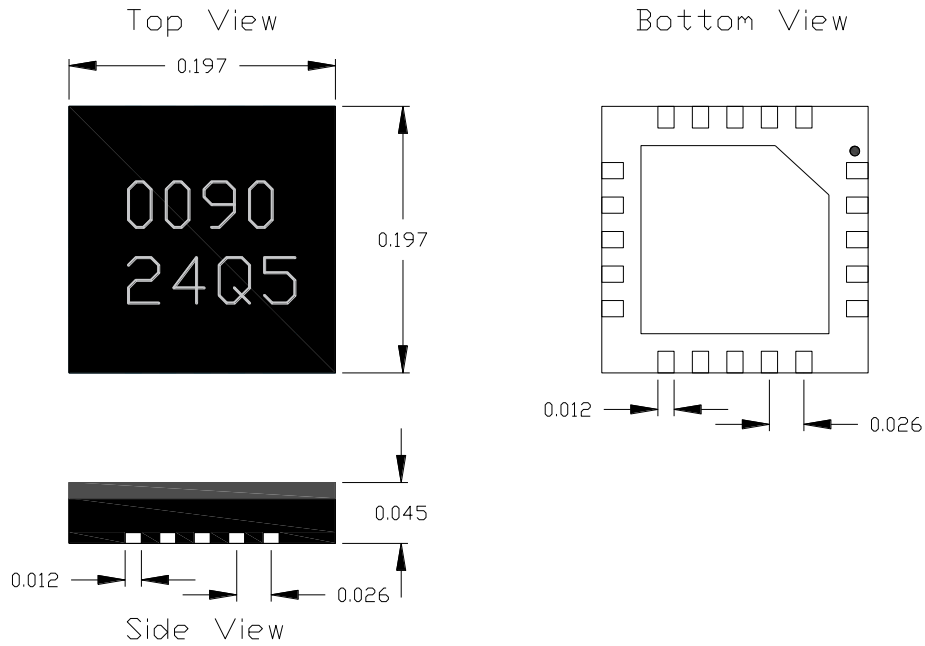


C) Power at $V_{dd} = +12V$ & $I_{dq} = 250mA$

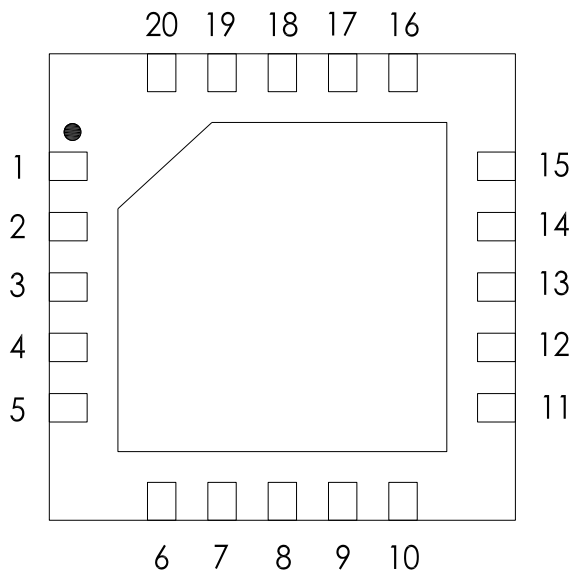


* Power measured using bias tee at the output for DC block. MMIC could be operated at lower than $V_{dd}=+12V$ or & $I_{dq} = 150mA$ with reduced power output.

PACKAGE OUTLINE



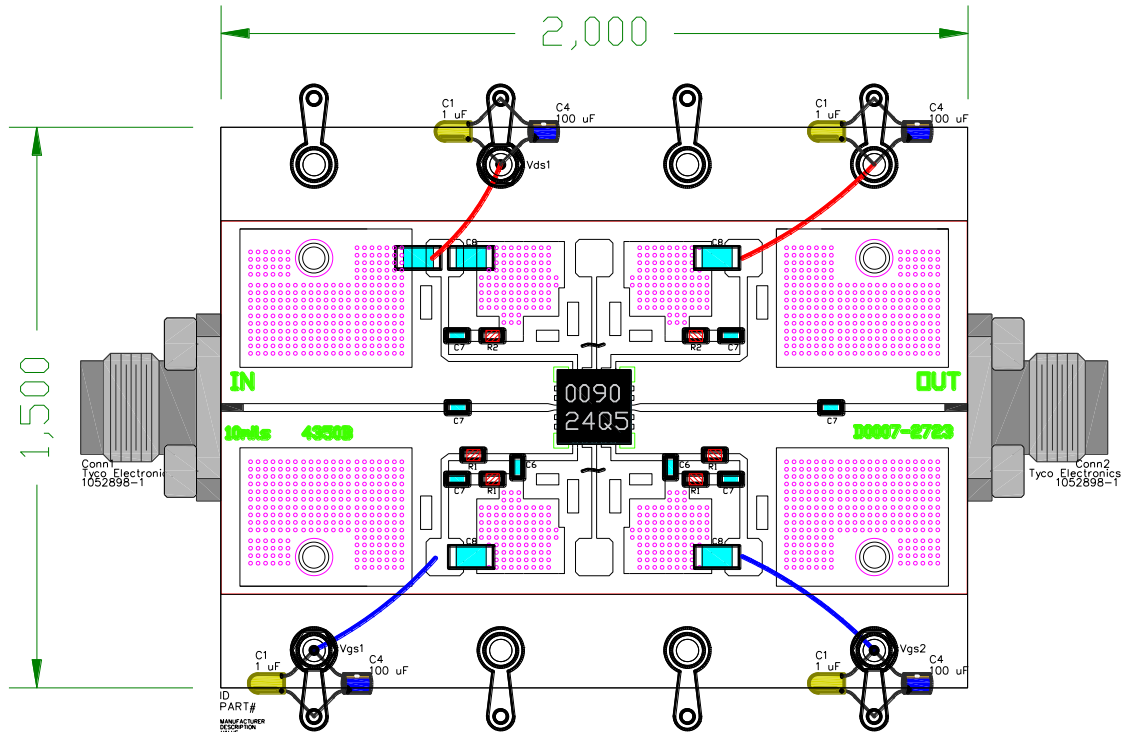
Pin Layout



Pin No.	Function	Bias
1, 2	NC	
3	RF in	DC Block
4,5	NC	
6	Vgs1	-0.7V
7,8	NC	
9	Vgs2	-0.7V
10,11,12	NC	
13	RF out	DC Block
14,15,16	NC	
17	Vdd2	+12V
18,19	NC	
20	Vdd1	+12V

- Gate biases are for reference only and may vary from lot to lot

TEST CIRCUIT for QFN Package



- Notes:
- 1- 10mils Rogers 4350B Material epoxied
 - 2- Ckt is for matched MMICs
 - 3- C6=20pf, C7=1000pF, C8=10uF
R1=50 Ohms, R2=10 Ohms
 - 4- All Caps & Resistors are 0603 size except for C8: 1206 size
 - 5- Bias tee should be used at output.
 - 6- Unused bias lines should be cut to avoid ripples and resonance
 - 7- Test Block is D0007-2004

Important Notes:

- 1- Recommended current biases are 100mA and 150mA for the first stage and second stage respectively for maximum output power. Gate biases of -0.7V are for reference only. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively.
- 2- For best noise figure use 75mA for first stage and 75mA for second stage.
- 3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2} .
- 4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 0.5mA & 1mA respectively at P_{1dB} .
- 5- External 1 μ F dipped tantalum capacitor should be attached to V_{dd1} and $V_{gs1,2}$ to decouple external bias leads.
- 6- DC block needed at input and the output.