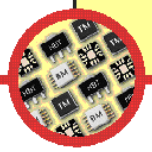
1Watt 0.05 – 9.5 GHz GaAs MMIC Power Amplifier

AM009530WM-QN5-R
March 2020
Rev 0



DESCRIPTION

AMCOM's AM009530WM-QN5-R is an ultra-broadband GaAs MMIC power amplifier. It has 20dB gain, and 30dBm output power over the 0.05 to 9GHz band. This MMIC is in a QFN package with both RF and DC leads at the bottom level of the package to facilitate low-cost SMT assembly to the PC board. Vias under the MMIC ground pad should have low thermal resistance to dissipate the MMIC DC power. This MMIC is RoHS compliant. This MMIC can be used as a driver with good input and output return loss at low positive bias (i.e. V_{dd} = +6V) and as a 1W power amplifier at high positive bias (i.e. V_{dd} =+12V).

FEATURES

- Ultrawide bandwidth from 50MHz to 9.5GHz
- High output power, P1dB = 30dBm
- High gain, 20dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE * (Bias Conditions**: V_{dd} = +12V, I_{dq} = 300mA)

Parameters	Minimum	Typical **	Maximum
Frequency	0.1 – 8GHz	0.05 – 9.5GHz	
Small Signal Gain	16dB	20dB	24dB
Gain Ripple		± 3dB	± 4.0dB
P1dB @ 1GHz	29dBm	30dBm	
P1dB from 0.1 to 8GHz		> 27dBm	
Psat @ 1GHz	29dBm	30.5dBm	
Psat from 0.1 to 8.0GHz		> 28dBm	
IP3 @ 1GHz		48dBm	
Input Return Loss	10dB	12dB	
Noise Figure		6dB	7dB
Output Return Loss	5dB	7dB	
Thermal Resistance		17°C/W	

* Specifications subject to change without notice.

** Gate biases corresponding to above currents are V_{gs1}=-0.7V, I_{gs1} < 0.5mA, V_{gs2}=-0.7V, I_{gs2} < 1mA and may vary from lot to lot. Gate currents could reach above limits only near power saturation. DC block needed at input & bias tee at the output to provide V_{dd2} bias.

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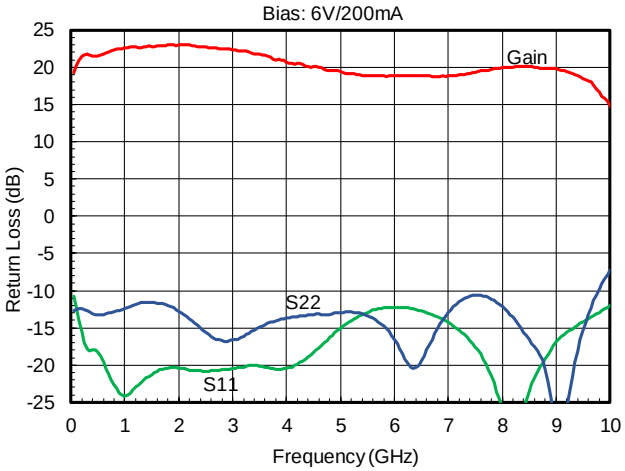
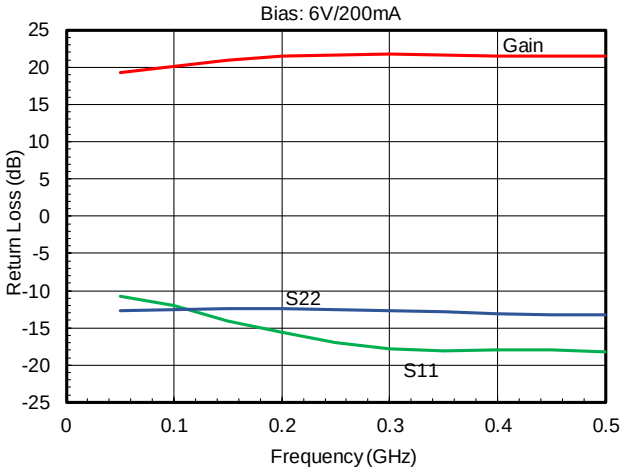
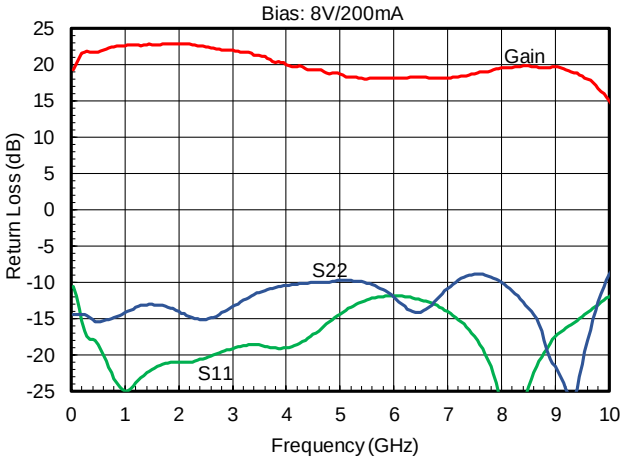
ABSOLUTE MAXIMUM RATING

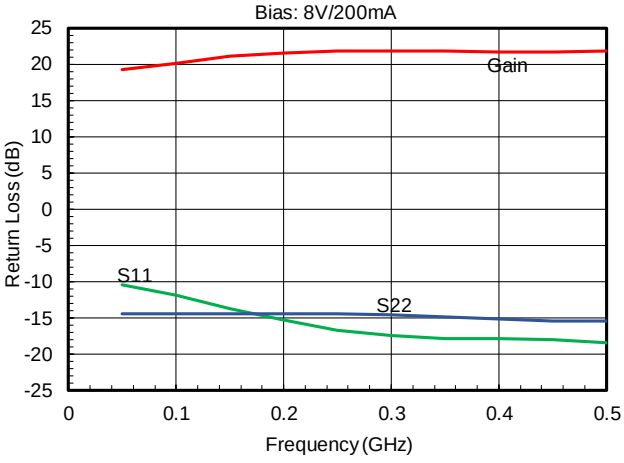
Parameters	Symbol	Rating
Drain source voltage	V_{dd}	13V
Gate source voltage	V_{gs1} & V_{gs2}	-5V
Drain source current	I_{dq1}	0.2A
Drain source current	I_{dq2}	0.40A
Continuous dissipation at 25ºC	P_t	7.8W
Channel temperature	T_{ch}	175°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

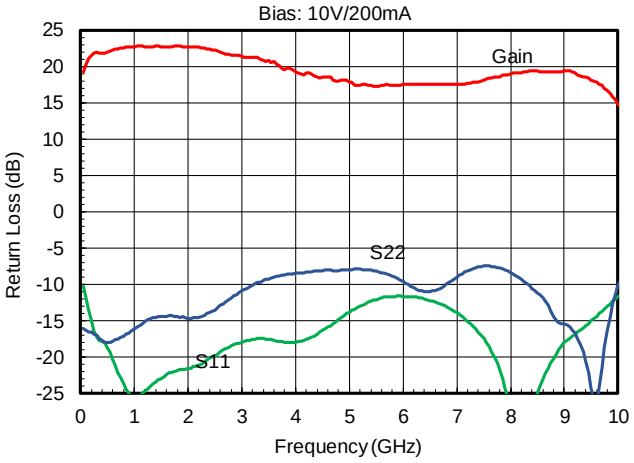
SMALL SIGNAL DATA*

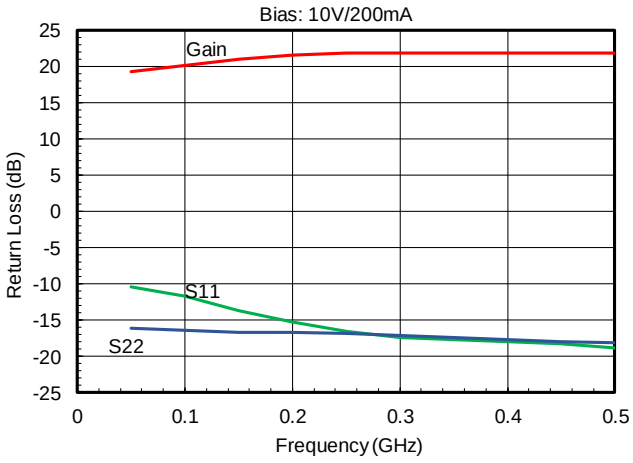


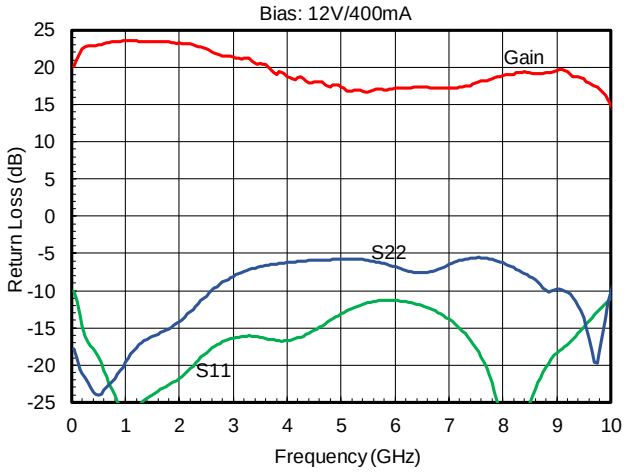


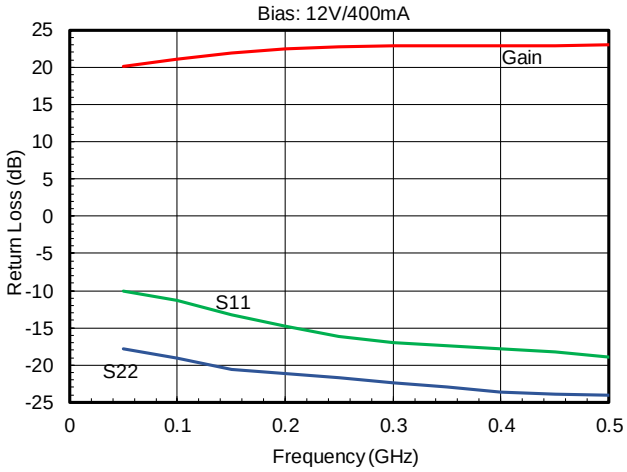






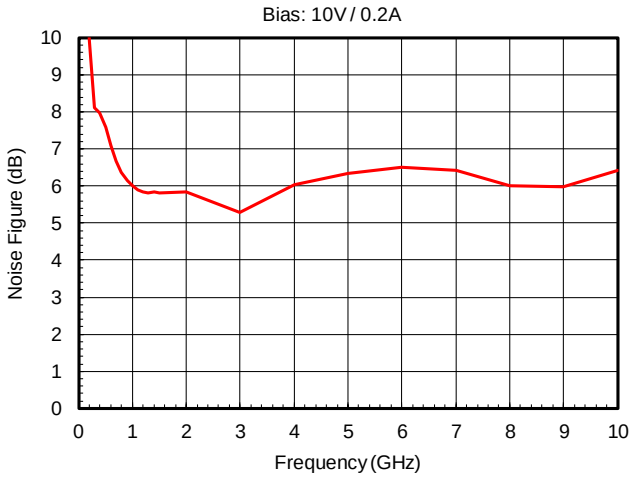




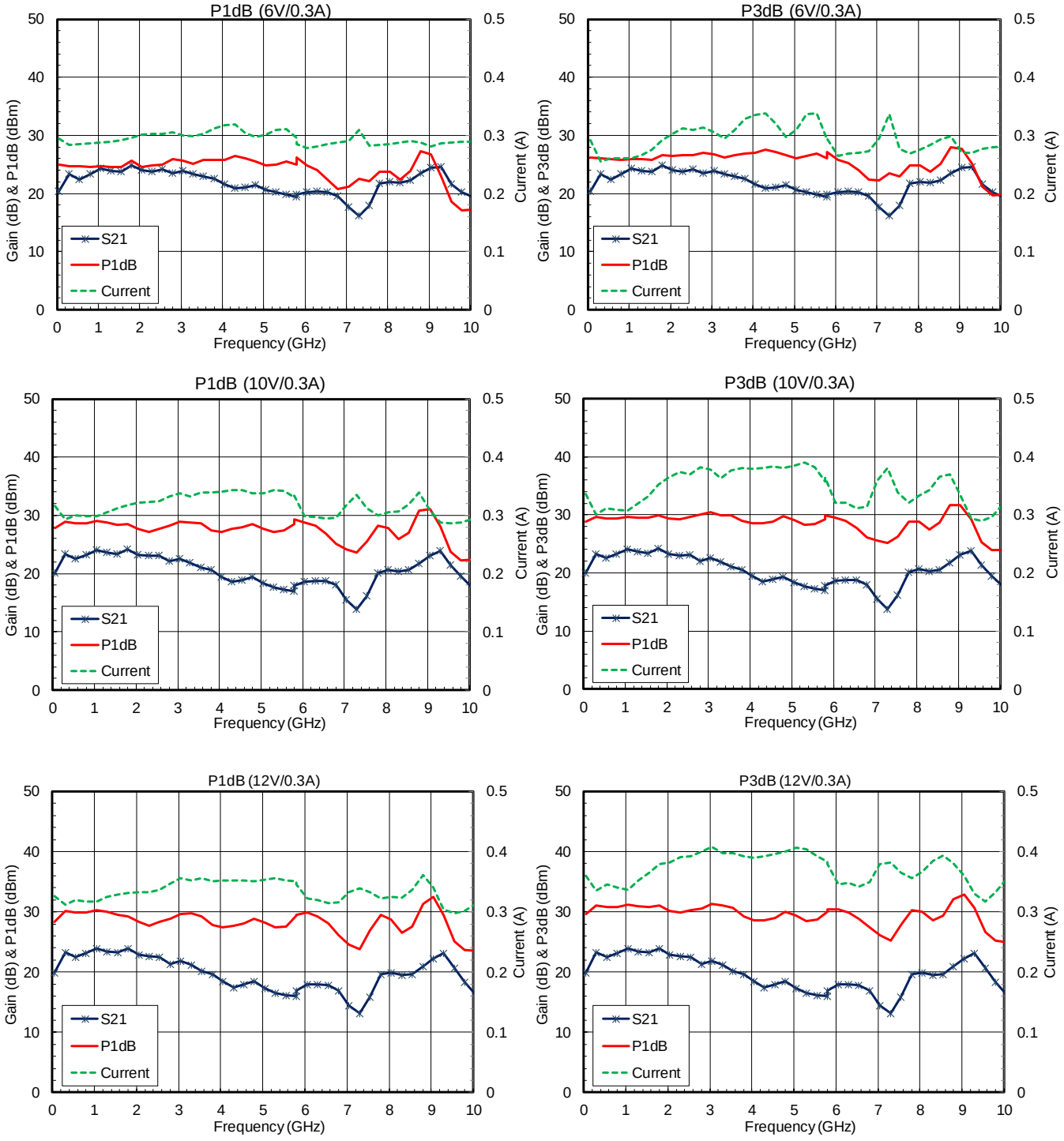


* S-Parameters measured using bias tee at the output. MMIC could be operated at lower than V_{dd}=+12V with almost same small signal parameters.

NOISE

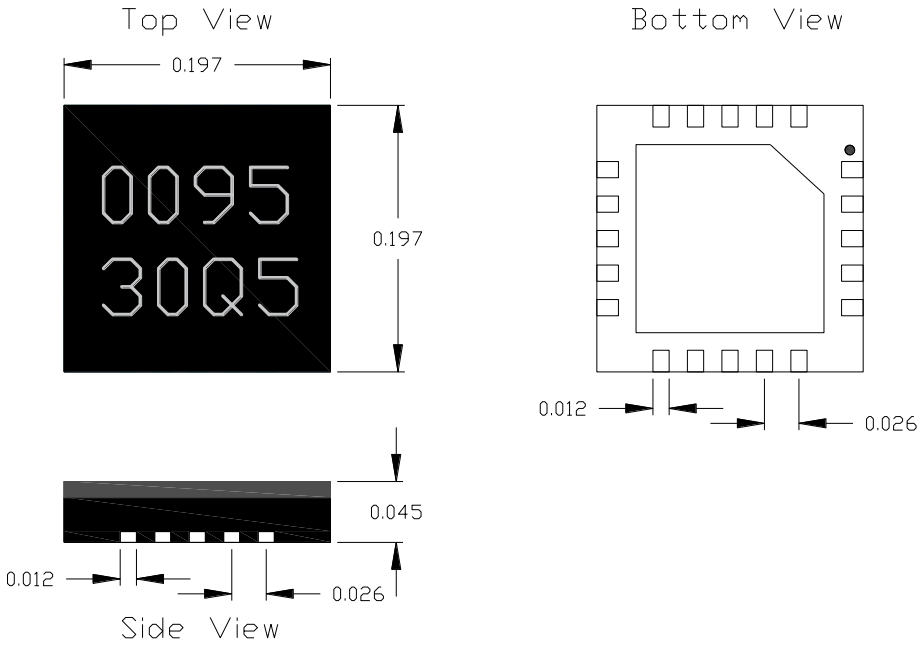


POWER DATA*

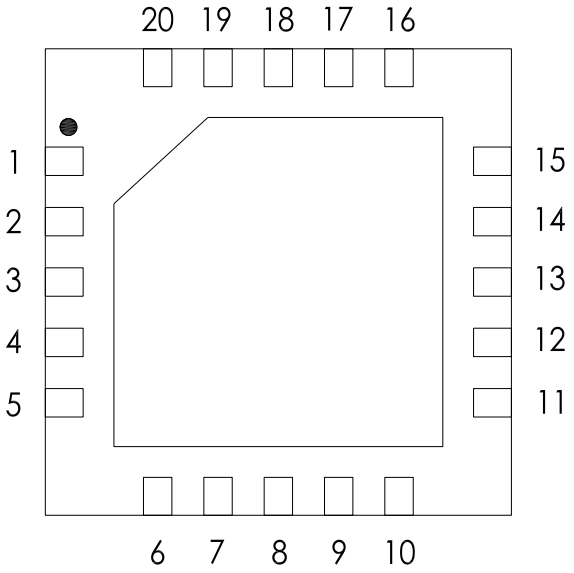


* Power measured using bias tee at the output. Variations in power with frequency is caused by VSWR of test setup.

PACKAGE OUTLINE



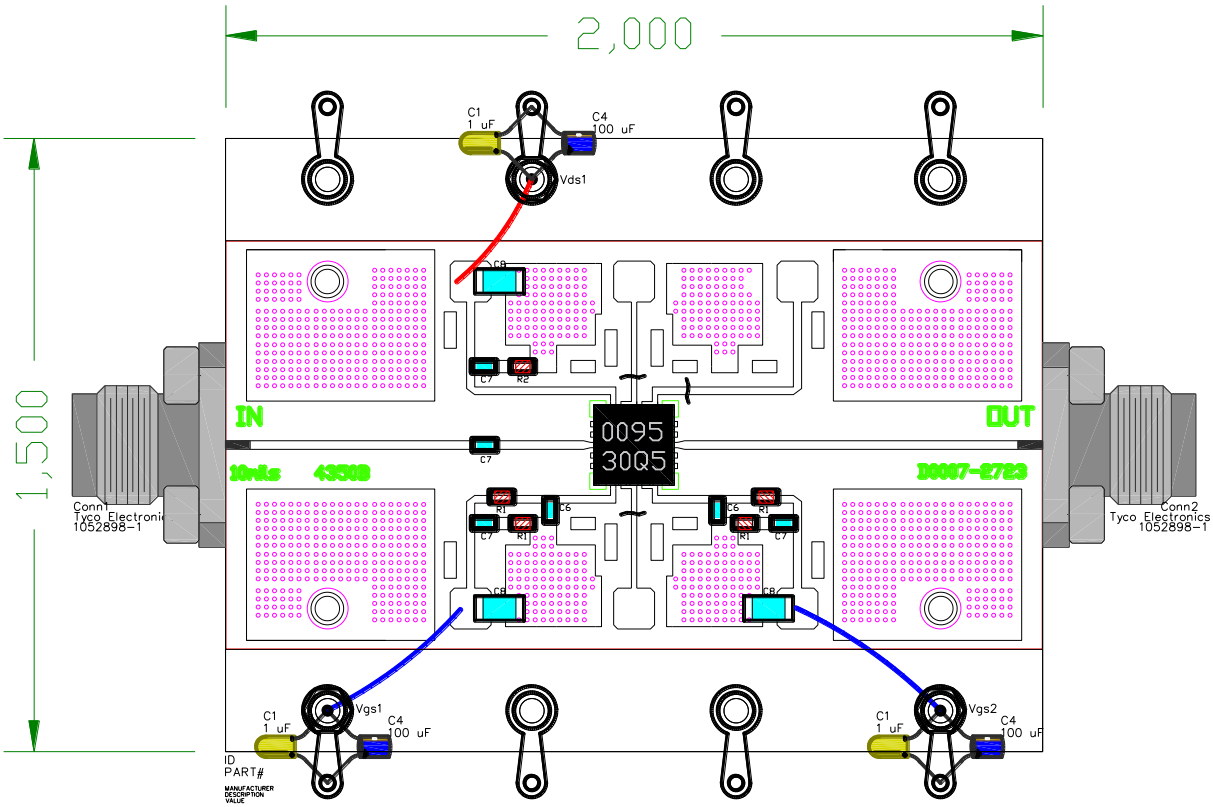
Pin Layout



Pin No.	Function	Bias
1, 2	NC	
3	RF in	DC Block
4,5	NC	
6	Vgs1	-0.7V
7,8	NC	
9	Vgs2	-0.7V
10,11,12	NC	
13	RF out & Vdd2	+12V
14,15,16	NC	
17	Vgs2	-0.7V
18,19	NC	
20	Vdd1	+12V

- Gate biases are for reference only and may vary from lot to lot

TEST CIRCUIT for QFN Package



Notes:
1- 10mils Rogers 4350B Material epoxied
2- Ckt is for matched MMICs
3- C6=20pf, C7=1000pF, C8=10uF
R1=50 Ohms, R2=10 Ohms
4- All Caps & Resistors are 0603 size except for C8: 1206 size
5- Bias tee should be used at output.
6- Unused bias lines should be cut to avoid ripples and resonance
7- Test Block is D0007-2004

Important Notes:

1- The +12V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).

2- Recommended current biases are 100mA and 200mA for the first stage and second stage respectively. Gate biases of -0.7V are for reference only. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively.

3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2}.

4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 0.5mA & 1mA respectively at P_{1dB}.

5- External 1 µF dipped tantalum capacitor should be attached to V_{dd1} and $V_{gs1,2}$ to decouple external bias leads.

6- DC block required at input & bias tee at the output.