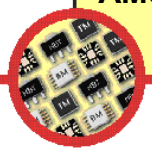
AMCOM COMMUNICATIONS
The RF Power House

GaAs MMIC Power Amplifier

AM012535MM-BM-R
AM012535MM-EM-R
AM012535MM-FM-R
April 2019
Rev 10



DESCRIPTION

AMCOM's AM012535MM-BM/EM/FM-R is part of the GaAs MMIC power amplifier series. It has 20dB gain and 33dBm output power over most of the 0.03 to 2.5GHz band. This MMIC is in a ceramic package with both RF and DC leads at the lower level of the package to facilitate low-cost SMT assembly to the PC board. When mounting directly to PCB, please see application note AN700 for instructions. This product is normally biased at 20V, but it works to as low as 6V with the same gain and reduced output power. Because of high DC power dissipation, we strongly recommend to mount these devices directly on a metal heat sink. The AM012535MM-FM-R is the AM012535MM-BM-R mounted on a gold plated copper flange carrier. The EM package has the same footprint as the FM package with straight leads and a Copper/Tungsten flange instead of the Copper flange. There are two screw holes on the flange to facilitate screwing on to a metal heat sink. This MMIC is RoHS compliant.

FEATURES

- Wide bandwidth from 0.03 to 2.5GHz
- High output power, P1dB = 33dBm
- High gain, 20dB
- Input & output 50-ohm impedance

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE*

(V_{dd} = +20V, I_{dd1} = 150mA, I_{dd2} = 400mA, V_{gg1} = -2.8V**, V_{gg2} = -0.9V** T_a = 25°C)

Parameters	Minimum	Typical	Maximum
Frequency	0.1 – 2.0GHz	0.03 – 2.5GHz	
Small Signal Gain	18dB	20dB	
Gain Ripple		± 1.0dB	± 2.0dB
P_{1dB} (0.1 to 2GHz)	32.0dBm	33.0dBm	
P_{sat} (0.1 to 2GHz)		33.5dBm	
Efficiency @ P_{1dB}		20%	
IP3 @ 1GHz		45dBm	
Input Return Loss	10dB	15dB	
Output Return Loss	6dB	10dB	
Thermal Resistance		4.7°C/W	

*Specifications subject to change without notice.
** V_{gg1} & V_{gg2} may vary from lot to lot

Performance at low DC bias voltages

Drain source voltage	Vds = 6V	Vds = 8V	Vds = 10V
Frequency Band	0.03 – 2.5GHz	0.03-2.5GHz	0.03-2.5GHz
Small Signal Gain	22dB	22dB	22dB
Output Power P1dB	23.5dBm	24dBm	24.2dBm

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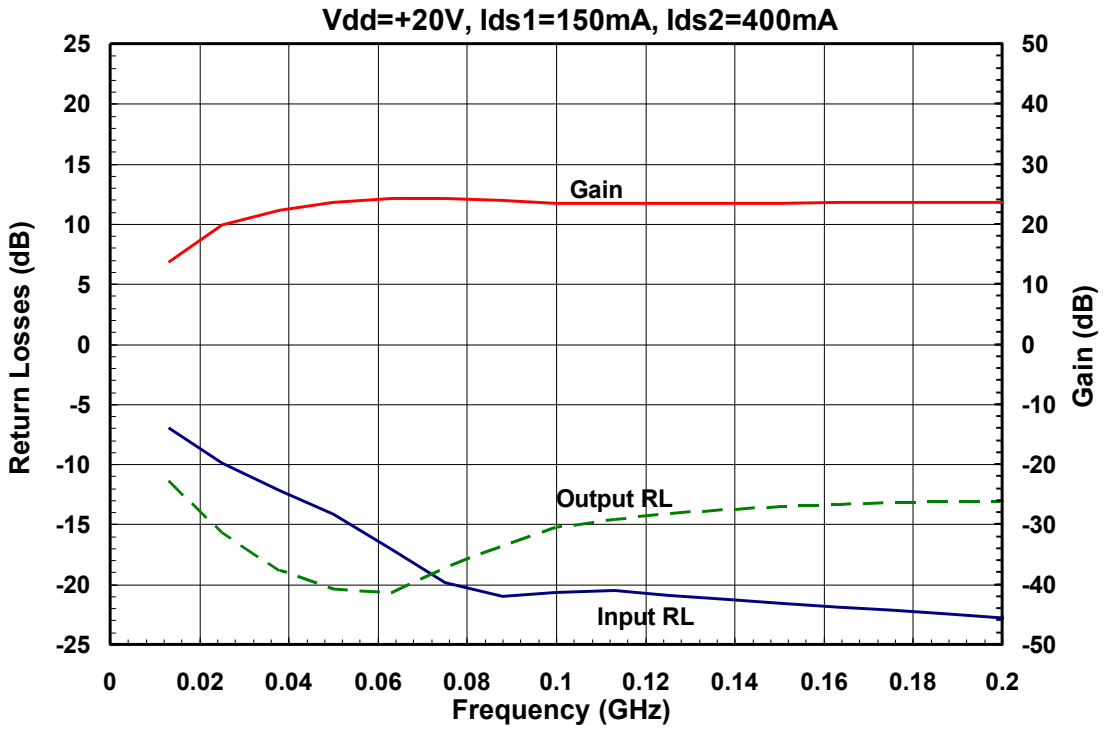
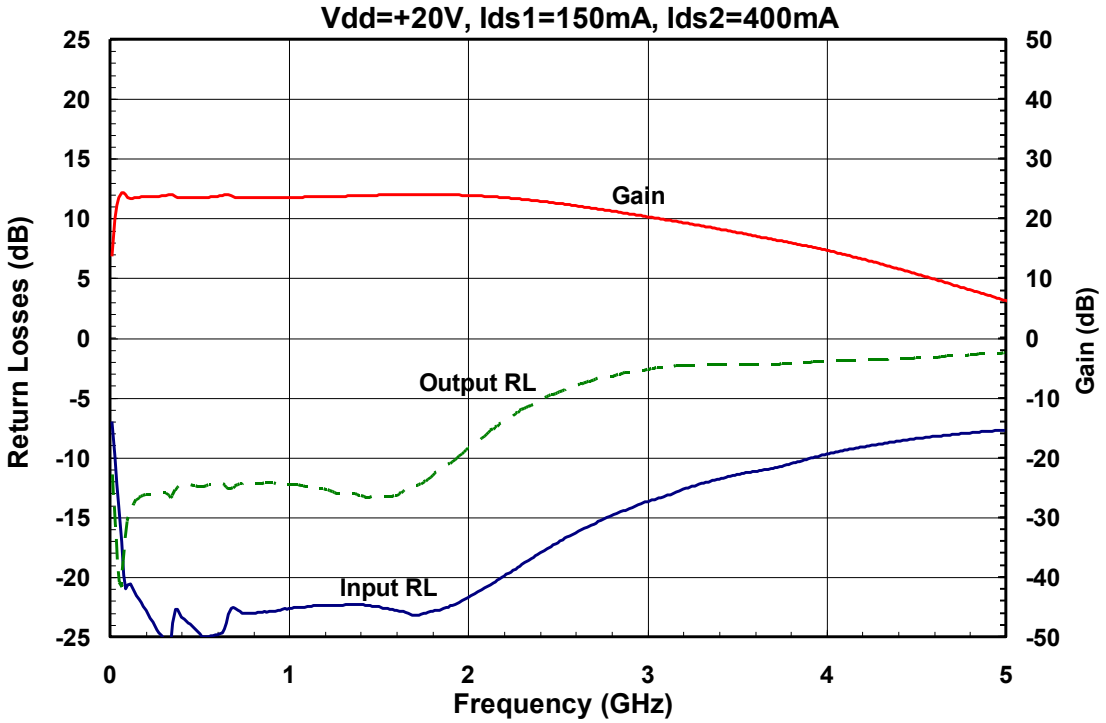
ABSOLUTE MAXIMUM RATING

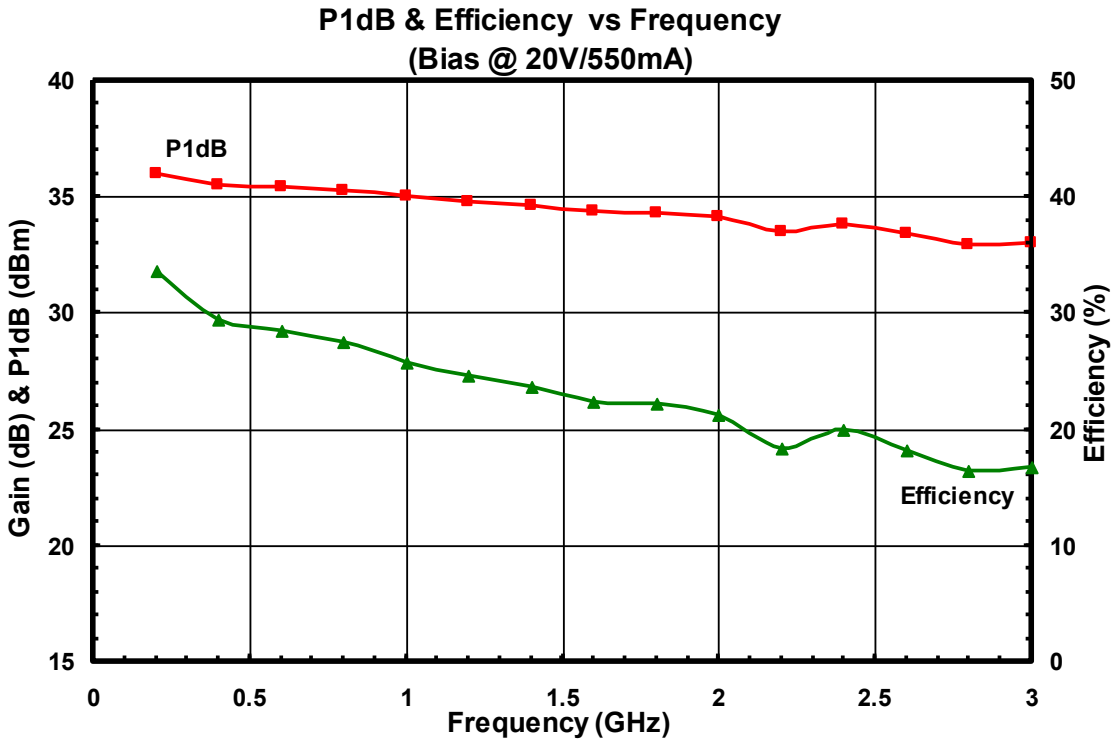
Parameters	Symbol	Rating
Drain source voltage	V_{dd}	24V
Gate source voltage	V_{gg1} , V_{gg2}	-8V
Drain source current	I_{dd1} +I_{dd2}	0.8A
Continuous dissipation at room temperature	P_t	18W
Channel temperature	T_{ch}	175°C
Storage temperature	T_{sto}	-55°C to +135°C

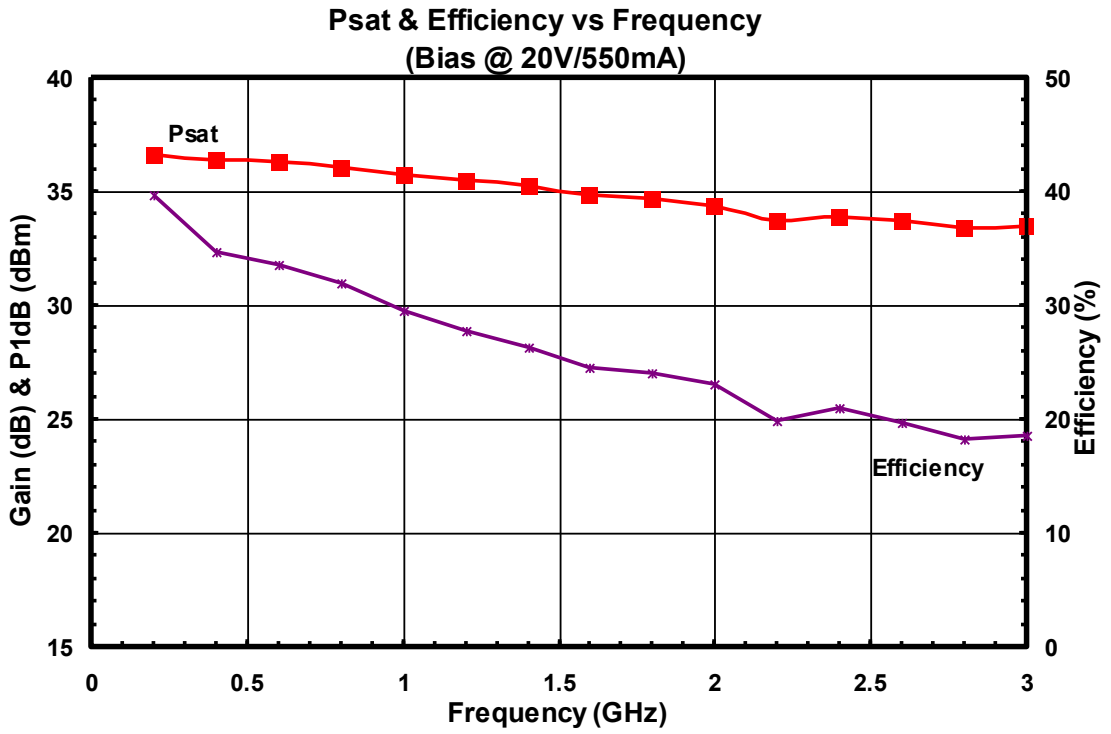
SMALL SIGNAL DATA (measurements performed with test fixture)

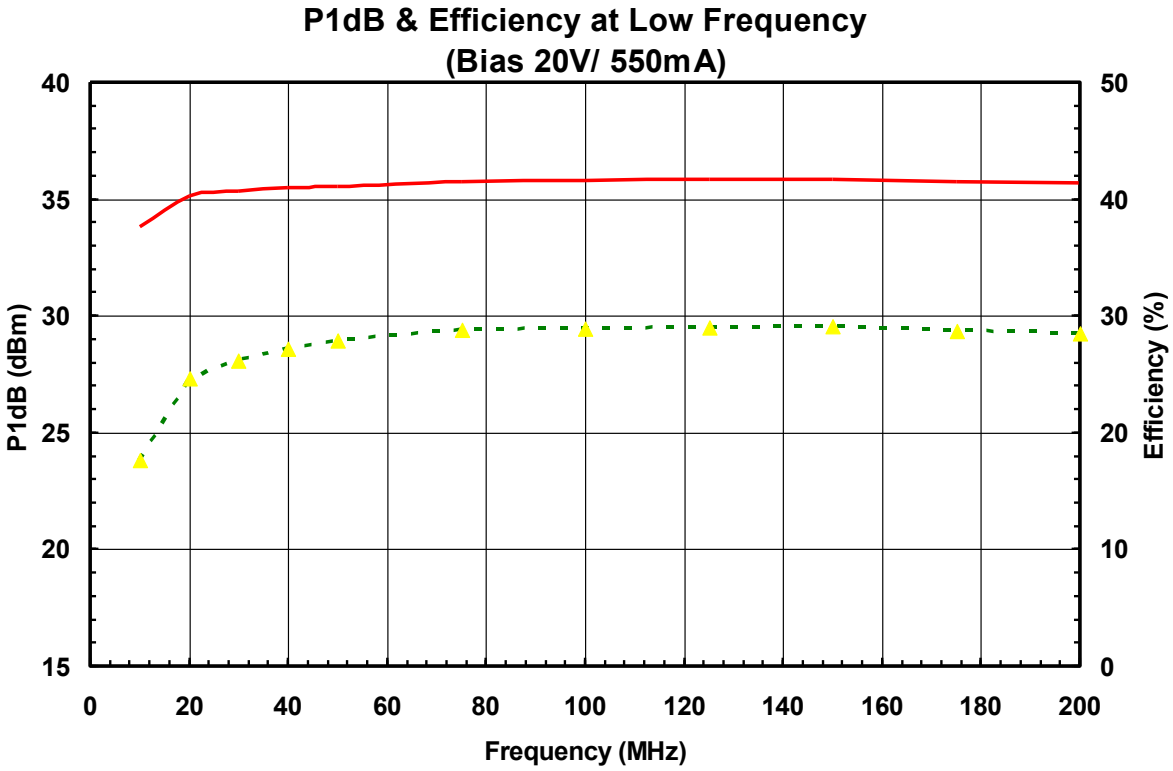


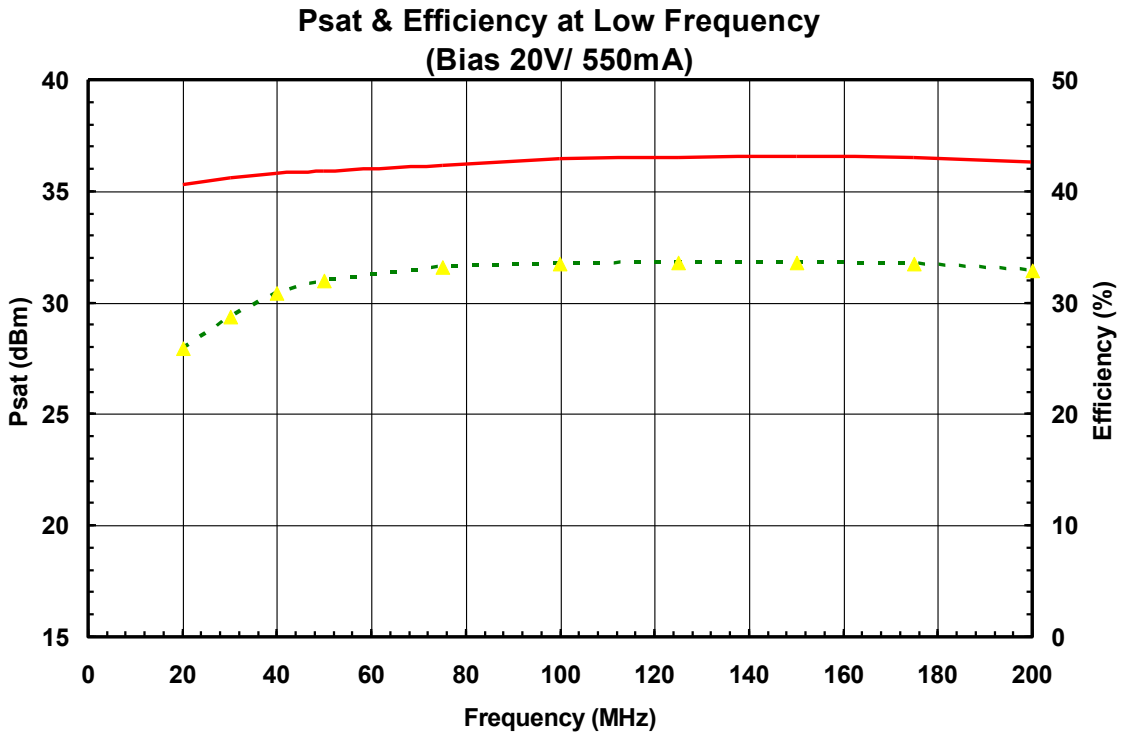


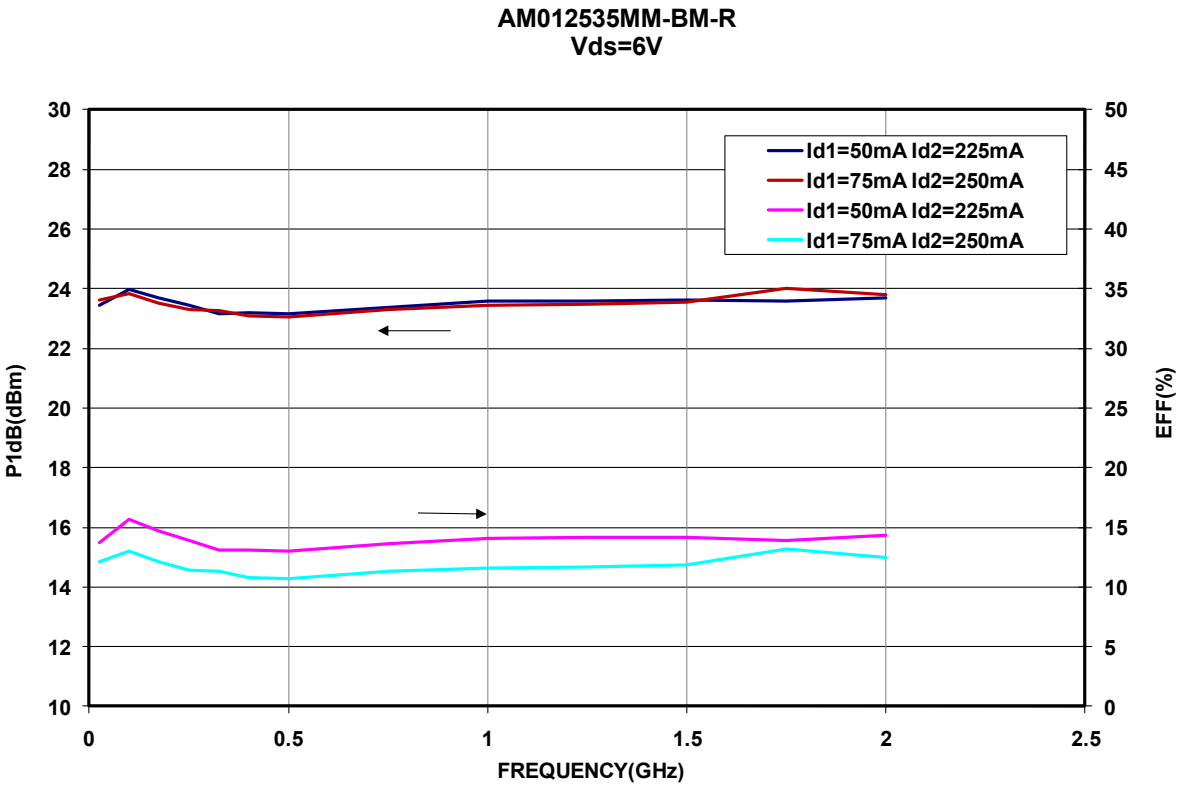
POWER DATA (Measurements performed with bias tee)

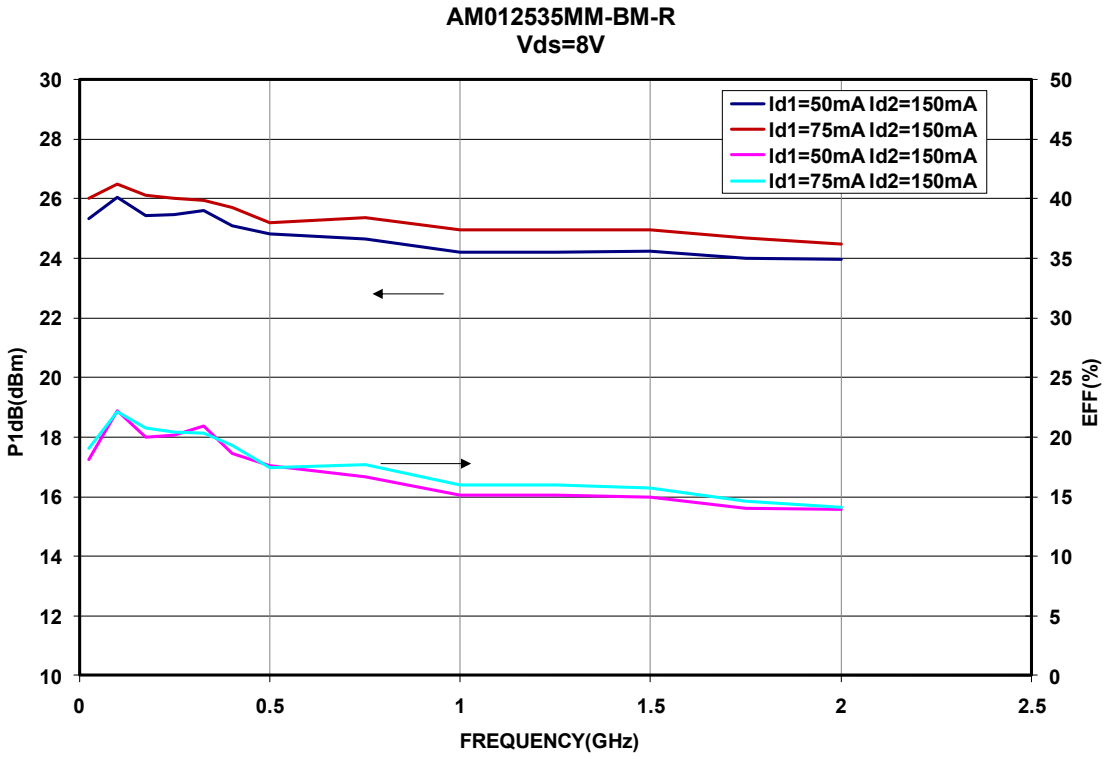


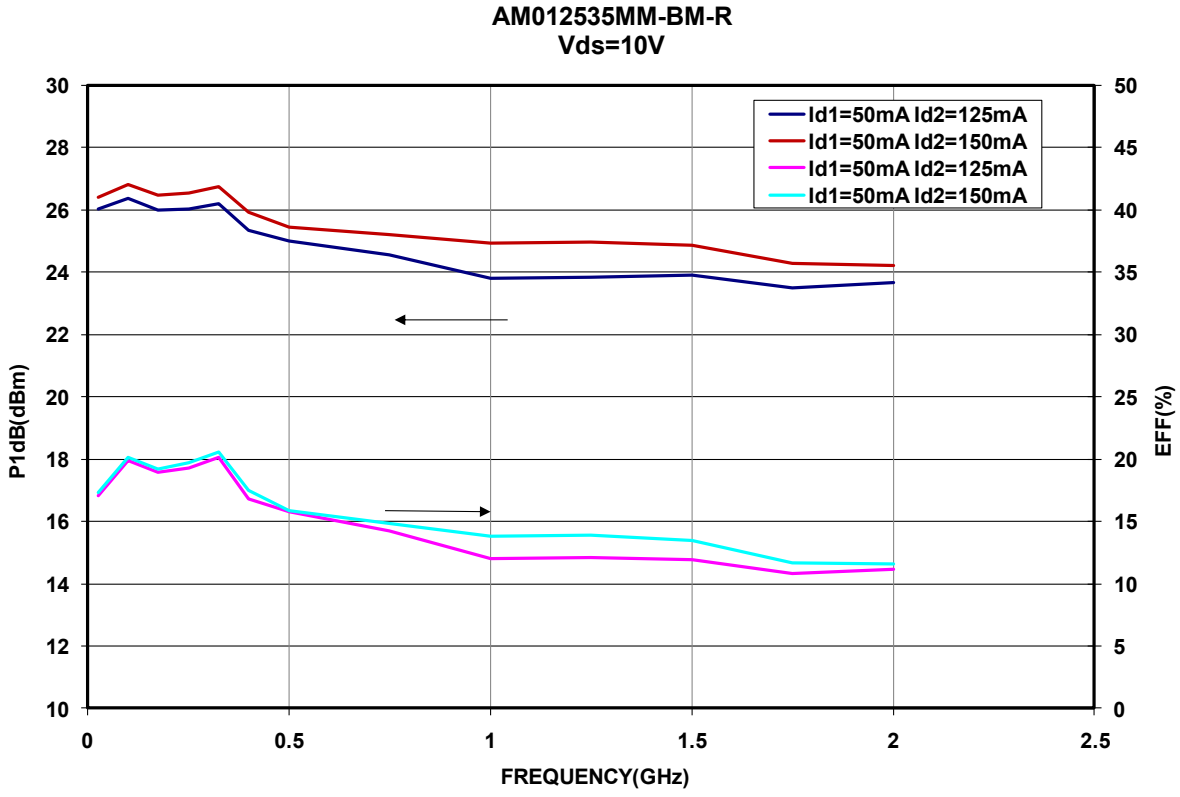

Psat & Efficiency vs Frequency
(Bias @ 20V/550mA)
Psat
Efficiency
Gain (dB) & P1dB (dBm)
Efficiency (%)
Frequency (GHz)
40
35
30
25
20
15
50
40
30
20
10
0
0
0.5
1
1.5
2
2.5
3


P1dB & Efficiency at Low Frequency
(Bias 20V/ 550mA)
P1dB (dBm)
Efficiency (%)
Frequency (MHz)
40
35
30
25
20
15
50
40
30
20
10
0
0
20
40
60
80
100
120
140
160
180
200

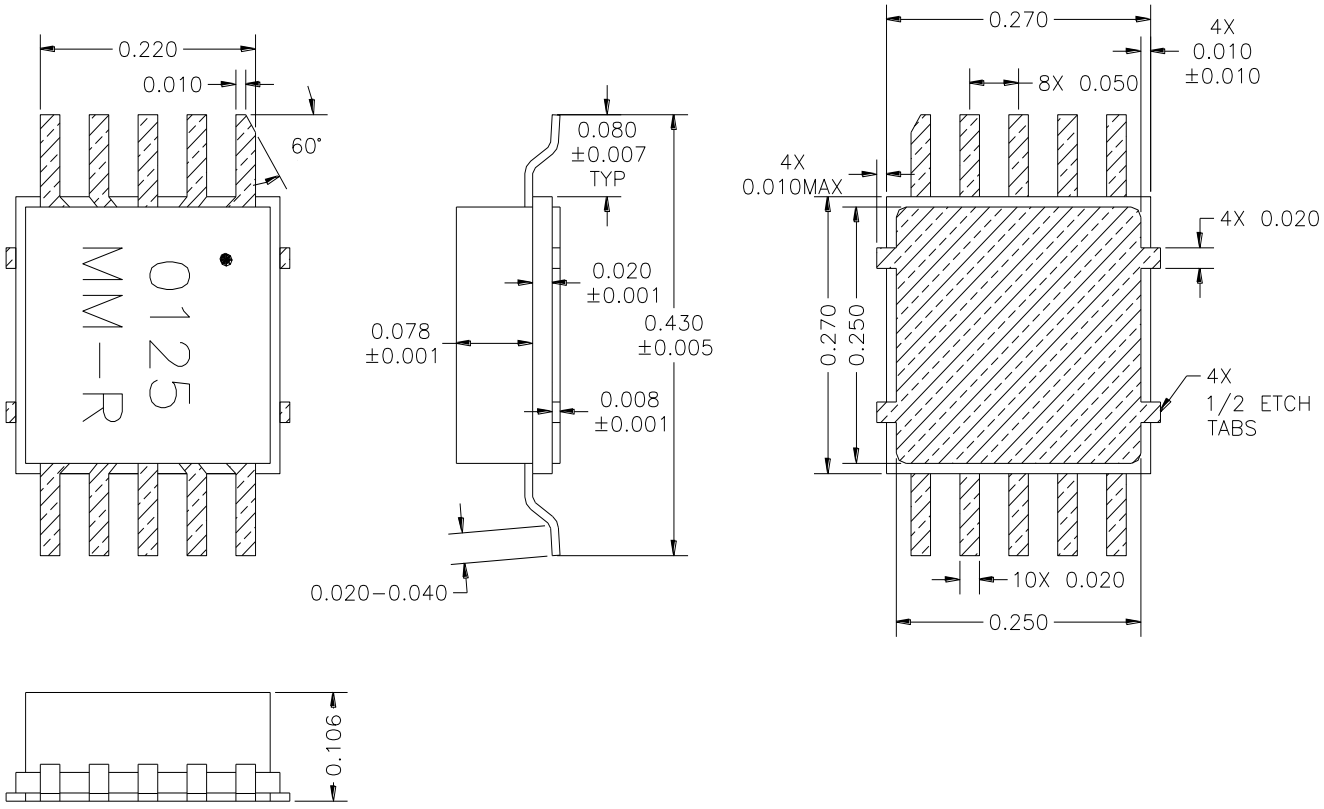

Psat & Efficiency at Low Frequency
(Bias 20V/ 550mA)
Psat (dBm)
Efficiency (%)
Frequency (MHz)
40
35
30
25
20
15
50
40
30
20
10
0
0
20
40
60
80
100
120
140
160
180
200


AM012535MM-BM-R
Vds=6V
Id1=50mA Id2=225mA
Id1=75mA Id2=250mA
Id1=50mA Id2=225mA
Id1=75mA Id2=250mA
P1dB(dBm)
EFF(%)
FREQUENCY(GHz)
30
28
26
24
22
20
18
16
14
12
10
50
45
40
35
30
25
20
15
10
5
0
0
0.5
1
1.5
2
2.5

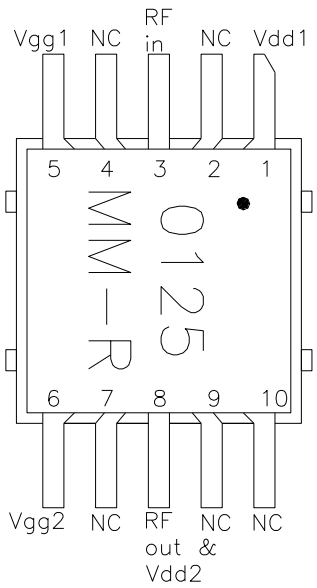

AM012535MM-BM-R
Vds=8V
Id1=50mA Id2=150mA
Id1=75mA Id2=150mA
Id1=50mA Id2=150mA
Id1=75mA Id2=150mA
P1dB(dBm)
EFF(%)
FREQUENCY(GHz)
30
28
26
24
22
20
18
16
14
12
10
50
45
40
35
30
25
20
15
10
5
0
0
0.5
1
1.5
2
2.5


AM012535MM-BM-R
Vds=10V
Id1=50mA Id2=125mA
Id1=50mA Id2=150mA
Id1=50mA Id2=125mA
Id1=50mA Id2=150mA
P1dB(dBm)
EFF(%)
FREQUENCY(GHz)
30
28
26
24
22
20
18
16
14
12
10
50
45
40
35
30
25
20
15
10
5
0
0
0.5
1
1.5
2
2.5

PACKAGE OUTLINE (BM)



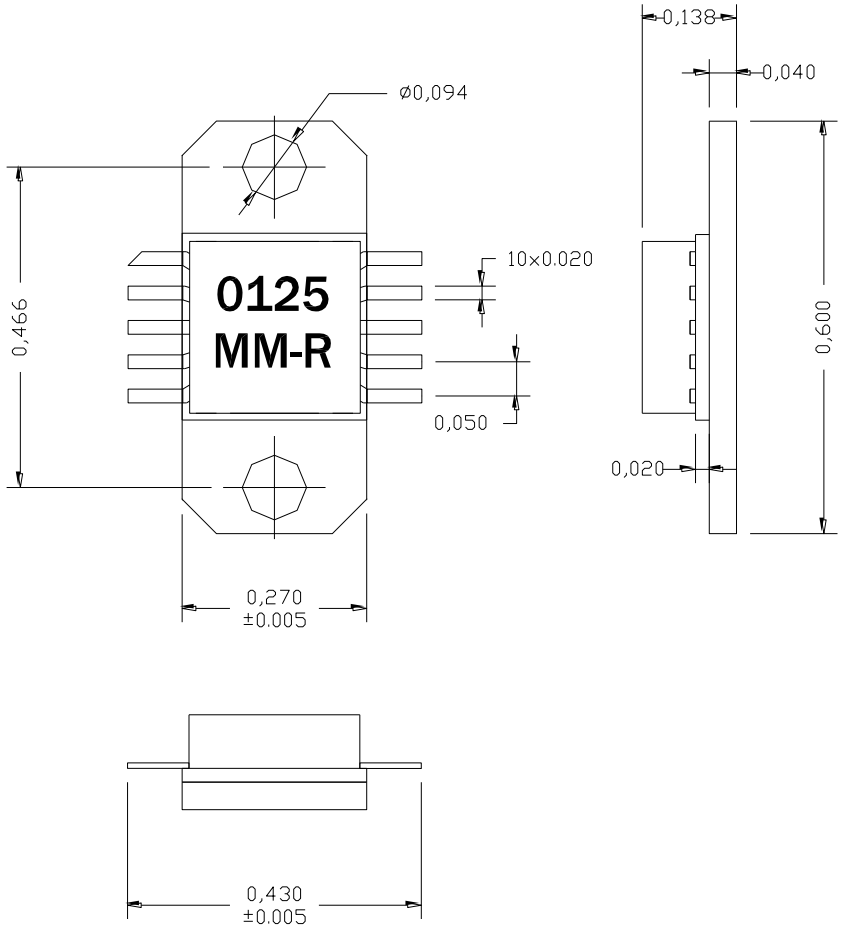
PIN LAYOUT



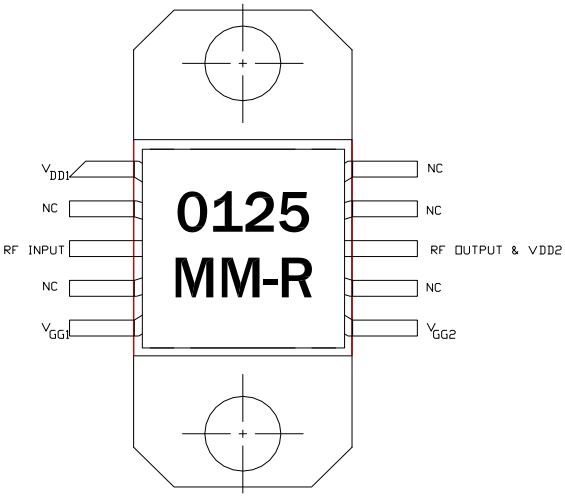
Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgg1	-2.8V
6	Vgg2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* V_{gg1} & V_{gg2} may vary from lot to lot

PACKAGE OUTLINE (EM)*



PIN LAYOUT

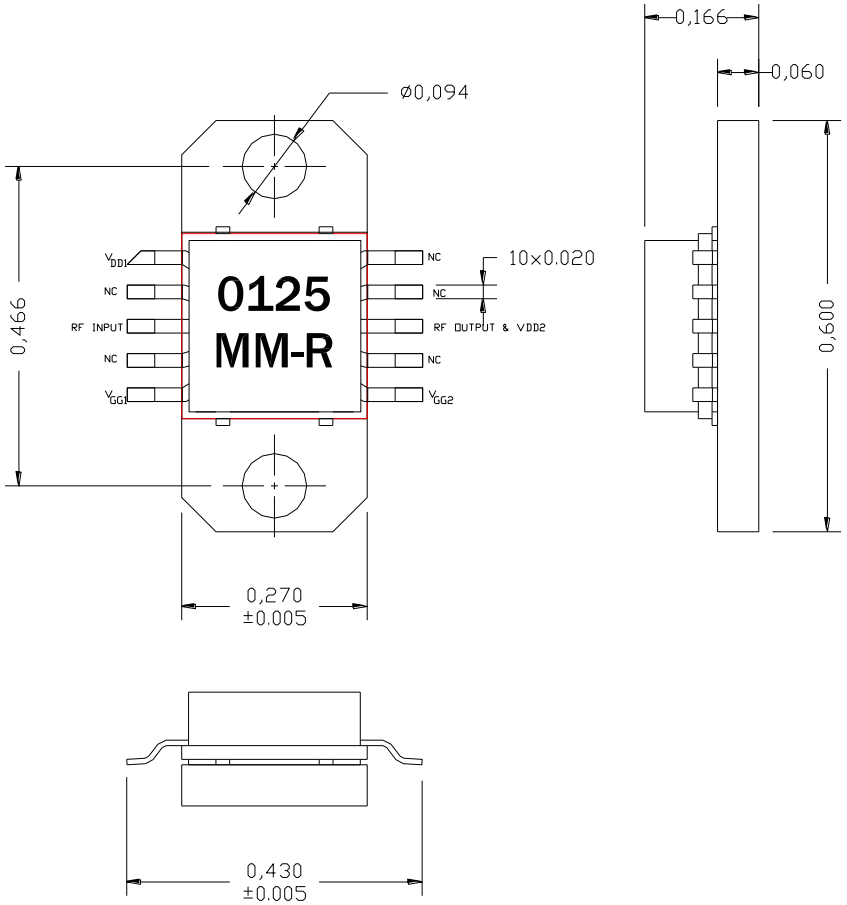


Pin No.	Function	Bias**
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgg1	-2.8V
6	Vgg2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

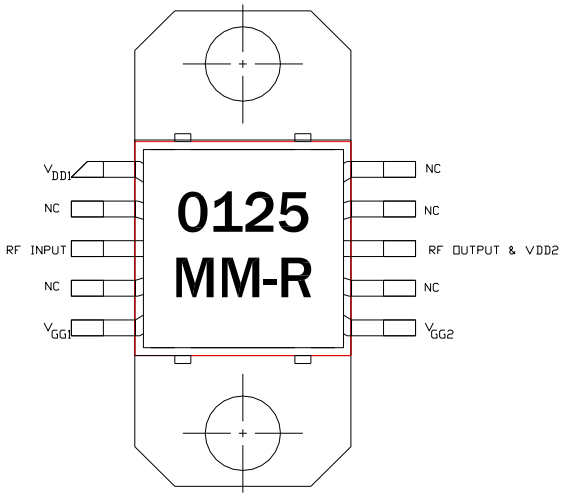
* EM version flange is made of CuW

** V_{gg1} & V_{gg2} may vary from lot to lot

PACKAGE OUTLINE (FM)*



PIN LAYOUT

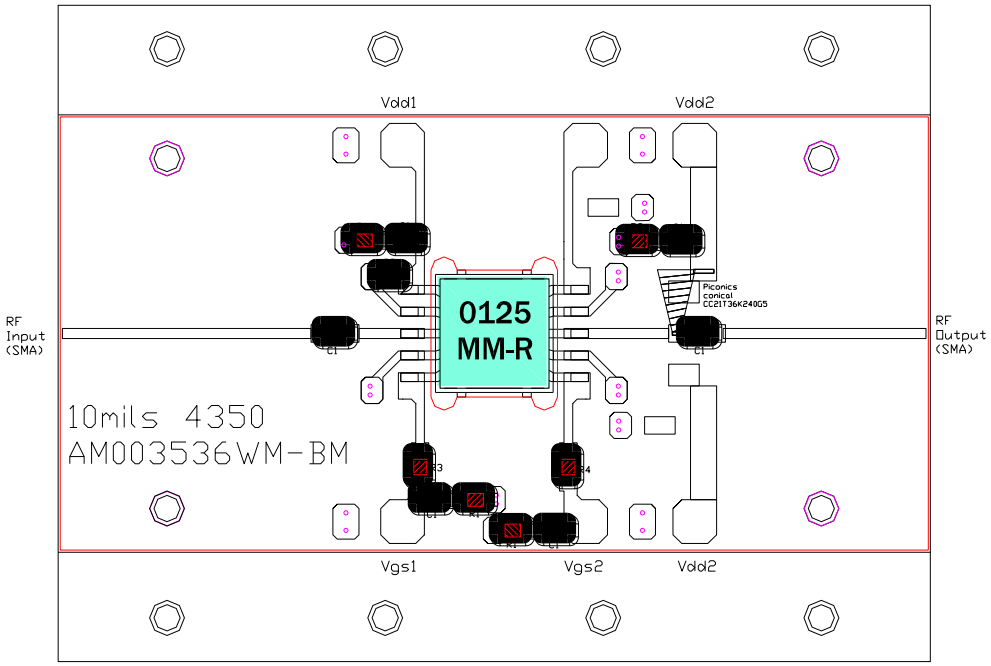


Pin No.	Function	Bias**
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgg1	-2.8V
6	Vgg2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* FM version flange is made of Copper

** V_{gg1} & V_{gg2} may vary from lot to lot

TEST CIRCUIT (BM)



IMPORTANT NOTES:

1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).

2- Recommended current biases are 150mA and 400mA for the first stage and second stage respectively. At V_{dd1} & V_{dd2} = +20V V_{gg1} & V_{gg2} values are around -2.8V and -0.9V respectively to obtain these desired currents but may vary from lot to lot. V_{gg1} & V_{gg2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively.

3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gg1} & V_{gg2}.

4- Due to direct DC connection between V_{dd1} & V_{gg1} pins through a large resistor there is a current around 10mA flowing out of the V_{gg1} pin. The current flowing out of the V_{gg2} pin is less than 100µA.

5- External 1 µF dipped tantalum capacitor should be attached to Vd and Vg to decouple external bias leads.

TEST CIRCUIT (EM & FM)