DESCRIPTION

AMCOM’s AM07512041WN-00 Chip is a broadband GaN MMIC power amplifier. It has 28dB gain, and 42 dBm output power over the 8.25 to 11.75 GHz band. This MMIC is matched to 50 Ohms.

FEATURES

- Broadband from 7.75 to 12.25GHz
- Saturated output power Psat is 42dBm
- High gain, 28dB
- Input & output matched to 50 Ohms

APPLICATIONS

- Instrumentation
- Commercial telecom transmission equipment
- Fixed microwave backhaul

TYPICAL PERFORMANCE *

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Minimum</th>
<th>Typical **</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>8.25 – 11.75 GHz</td>
<td>7.75 – 12.25GHz</td>
<td></td>
</tr>
<tr>
<td>Small Signal Gain</td>
<td>23dB</td>
<td>28dB</td>
<td></td>
</tr>
<tr>
<td>Gain Ripple</td>
<td>± 2</td>
<td>± 4.0dB</td>
<td></td>
</tr>
<tr>
<td>P1dB</td>
<td>35dBm</td>
<td>38 dBm</td>
<td></td>
</tr>
<tr>
<td>Psat</td>
<td>39 dBm</td>
<td>42 dBm</td>
<td></td>
</tr>
<tr>
<td>Psat Efficiency</td>
<td>27%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise Figure</td>
<td>TBD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP3 dBm</td>
<td>47</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>15dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>7dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>TBD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Specifications subject to change without notice.
** Bias Conditions**: V_{ds1, 2, 3} = +28V, I_{dsq1, 2} = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3} = -1.8V.
ABSOLUTE MAXIMUM RATING

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>First &amp; second stage drain voltages</td>
<td>V_{ds1}, V_{ds2}</td>
<td>32V</td>
</tr>
<tr>
<td>Third stage drain voltage</td>
<td>V_{ds3}</td>
<td>32V</td>
</tr>
<tr>
<td>Gate source voltage</td>
<td>V_{gs1}, V_{gs2}, V_{gs3}</td>
<td>-6V</td>
</tr>
<tr>
<td>Drain source current</td>
<td>I_{dsq1} + I_{dsq2}</td>
<td>1A</td>
</tr>
<tr>
<td>Drain source current</td>
<td>I_{dsq3}</td>
<td>1.5A</td>
</tr>
<tr>
<td>Continuous dissipation at 25°C</td>
<td>P_{t}</td>
<td>80W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>T_{ch}</td>
<td>200°C</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>T_{op}</td>
<td>-55°C to +85°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>T_{sto}</td>
<td>-55°C to +135°C</td>
</tr>
</tbody>
</table>

SMALL SIGNAL DATA*

* S-Parameters measured using test fixture. Bias Conditions**: V_{ds1, 2, 3} = +28V, I_{dsq1+2} = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3} = -1.8V.

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* Parameters measured using test fixture. Bias Conditions**: V_{ds1, 2, 3} = +28V, I_{dsq1+2} = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3} = -1.8V.
POWER DATA (Recommended bias conditions)

28V/650mA/900mA

- P5dB (dBm)
- PAEF

Efficiency %

P5dB (dBm)
Frequency (GHz)

28V/650mA/900mA

- P1dB (dBm)
- PAEF

Efficiency %

P1dB (dBm)
Frequency (GHz)
POWER DATA vs \( V_{dd} \)

- **Psat @ 28V**
- **Psat @ 24V**
- **Psat @ 20V**
- **PAE @ 28V**
- **PAE @ 24V**
- **PAE @ 20V**

- **SSG @ 28V**
- **SSG @ 24V**
- **SSG @ 20V**

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**Frequency (GHz)**

1. **Psat (dBm)**
2. **PAE %**
3. **SSG (dB)**
Notes:

1) Dimensions in millimeter
2) Chip is 4x3.8 mm
3) RF bond pads are 140X180 microns, 50 ohms matched, and DC blocked.
4) Drains and Gates pads are all 200x200 microns
5) Use eutectic perform for ship assembly

<table>
<thead>
<tr>
<th>Bond Pad #</th>
<th>Symbol</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vgs1</td>
<td>-1.8V</td>
</tr>
<tr>
<td>2</td>
<td>RF in</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>Vds1</td>
<td>+28V</td>
</tr>
<tr>
<td>4</td>
<td>Vgs2</td>
<td>-1.8V</td>
</tr>
<tr>
<td>5</td>
<td>Vds2</td>
<td>+28V</td>
</tr>
<tr>
<td>6</td>
<td>Vgs3</td>
<td>-1.8V</td>
</tr>
<tr>
<td>7</td>
<td>Vds3</td>
<td>+28V</td>
</tr>
<tr>
<td>8</td>
<td>RF out</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>Vds3</td>
<td>+28V</td>
</tr>
<tr>
<td>10</td>
<td>Vgs3</td>
<td>-1.8V</td>
</tr>
<tr>
<td>11</td>
<td>Vds2</td>
<td>+28V</td>
</tr>
<tr>
<td>12</td>
<td>Vgs2</td>
<td>-1.8V</td>
</tr>
</tbody>
</table>
CIRCUIT SCHEMATIC

Vgs

1 uF

RF in

1000 pF

50 ohms

1000 pF

1000 pF

10 ohms

50 ohms

RF out

Vds

1 uF

1000 pF

50 ohms

1000 pF

1000 pF

10 ohms

50 ohms

Vgs

1 uF

1000 pF

50 ohms

1000 pF

1000 pF

10 ohms

50 ohms
TEST CIRCUIT

Notes:
1- Use epoxy to mount PCB, and Eutectic soldering to mount chip
2- C1=1uF(Dipped Radial Tantalum), C4=100uF(Aluminum Electrolytic)
   C2=1000pF, C3=20pF , R1=50ohms, R2=10ohms, R3=5ohms
3- All SMT Caps & Resistors are 0402 size

Important Notes:

1- Recommended current biases are 220mA for first, 430mA for second stage and 900mA for the third stage.
   Gate biases of 1.8V are for reference only. Gate voltages could be adjusted to vary the currents going thru
   drain pins.
2- Do not apply drain voltages without proper negative voltages on gates. Otherwise MMIC would fail due to
   excess heat.
3- Eutectic soldering is recommended for chip mounting
4- AutoCAD DXF file is available