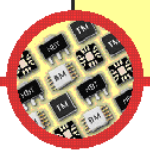
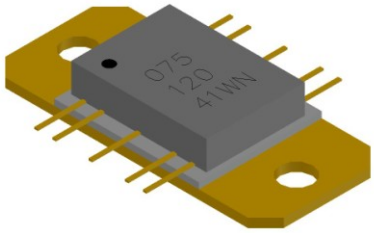
Gallium Nitride MMIC 15W 7.75 – 12.25 GHz Power Amplifier

AM07512041WN-SN-R
December 2019
Rev 0



DESCRIPTION

The AM07512041WN-SN-R is in a ceramic package with a flange and straight RF and DC leads for drop-in assembly. It has 27dB gain, and 41dBm output power over the 8.25 to 11.75 GHz band. Because of high DC power dissipation, good heat sinking is required. The package is RoHS compliant. This MMIC is matched to 50 Ohms.



FEATURES

- Broadband from 7.75 to 12.25GHz
- Saturated output power Psat is 42dBm
- High gain, 28dB
- Input & output matched to 50 Ohms

APPLICATIONS

- Instrumentation
- Commercial telecom transmission equipment
- Fixed microwave backhaul

TYPICAL PERFORMANCE *

Parameters	Minimum	Typical **	Maximum
Frequency	8.25 – 11.75 GHz	7.75 – 12.25GHz	
Small Signal Gain	22dB	27dB	
Gain Ripple		± 2	± 4.0dB
P1dB	34.5 dBm	37.5 dBm	
Psat	38 dBm	41 dBm	
Psat Efficiency		22%	
Noise Figure		TBD	
IP3		46.5	
Input Return Loss		10dB	
Output Return Loss		7dB	
Thermal Resistance		TBD	

* Specifications subject to change without notice.

** Bias Conditions**: $V_{ds1, 2, 3}$ = +28V, $I_{dsq1, 2}$ = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3} =-1.8V.

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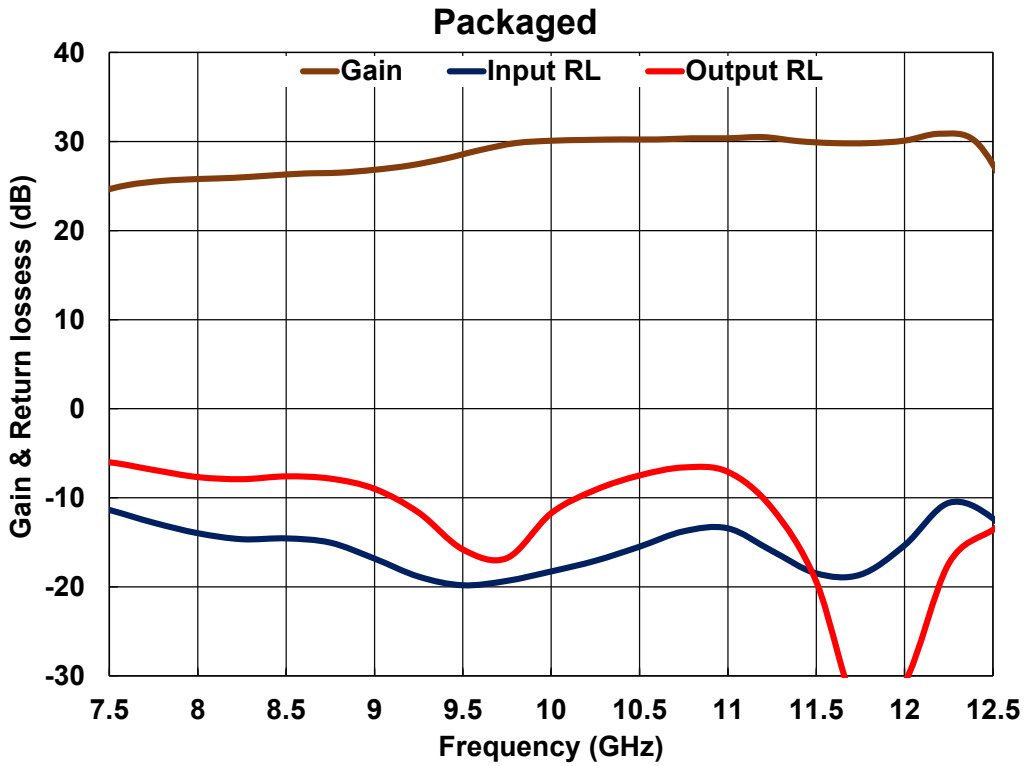
ABSOLUTE MAXIMUM RATING

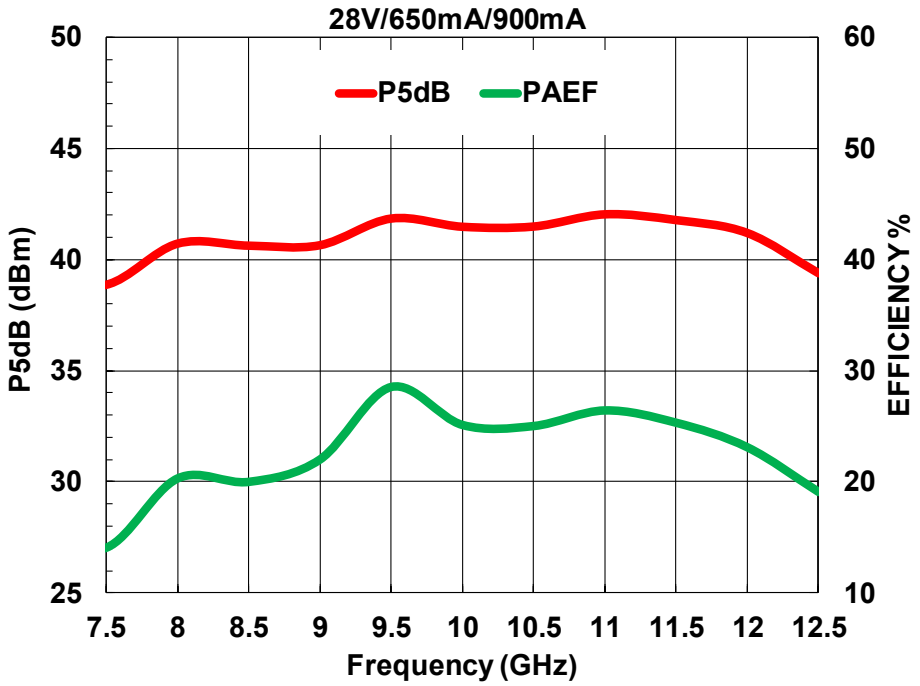
Parameters	Symbol	Rating
First & second stage drain voltages	V_{ds1} , V_{ds2}	32V
Third stage drain voltage	V_{ds3}	32V
Gate source voltage	V_{gs1}, V_{gs2}, V_{gs3}	-6V
Drain source current	I_{dsq1} + I_{dsq2}	1A
Drain source current	I_{dsq3}	1.5A
Continuous dissipation at 25ºC	P_t	80W
Channel temperature	T_{ch}	200°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

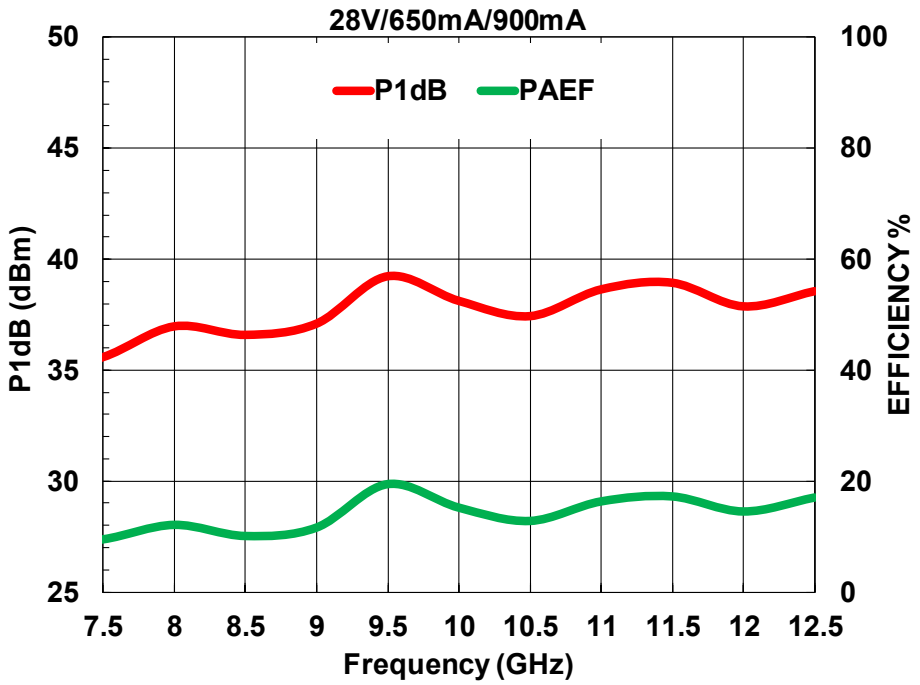
SMALL SIGNAL DATA*



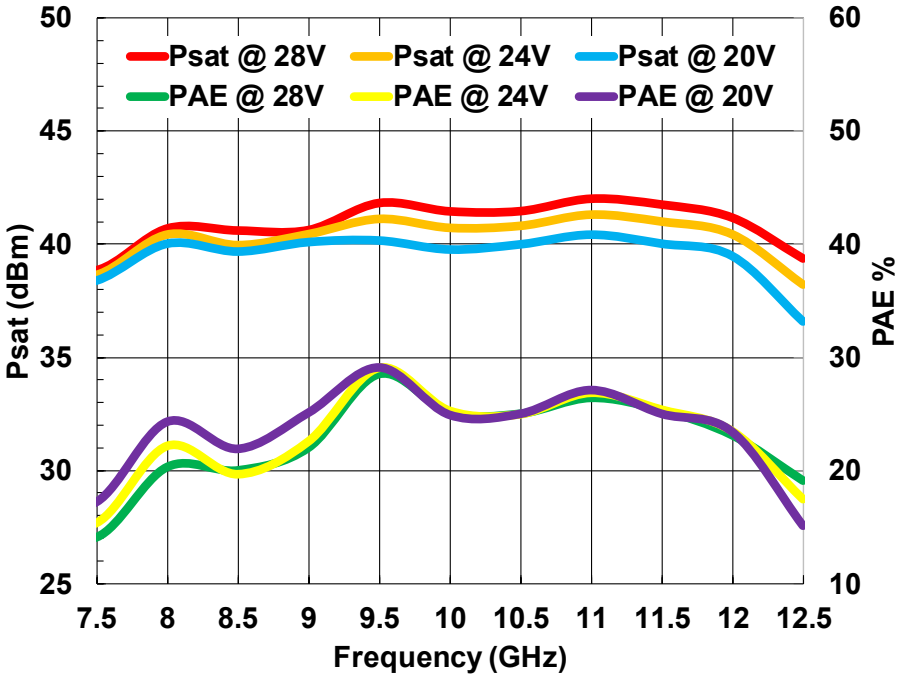
* S-Parameters measured using test fixture. Bias Conditions**: $V_{ds1,\,2,\,3}$ = +28V, I_{dsq1+2} = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3} =-1.8V.

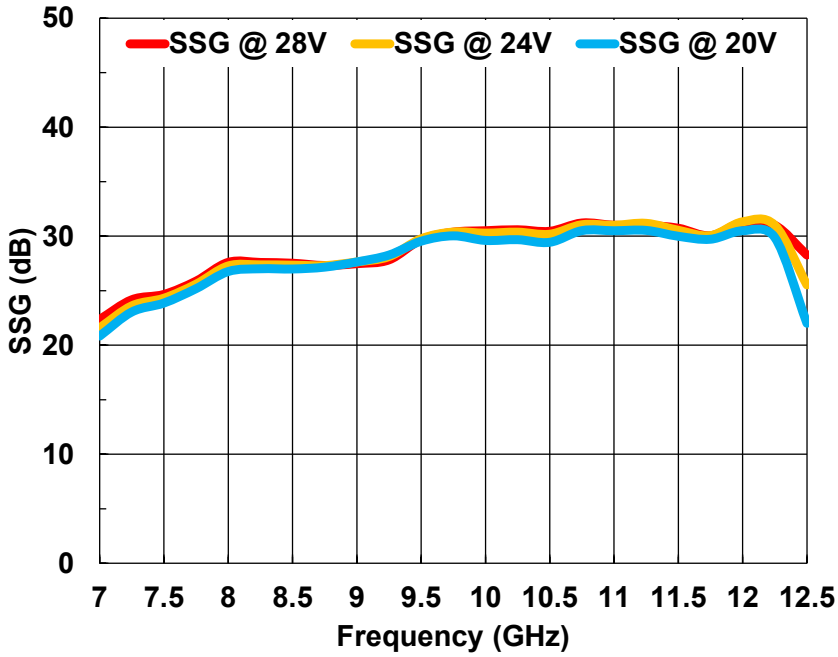
POWER DATA (Recommended bias conditions)





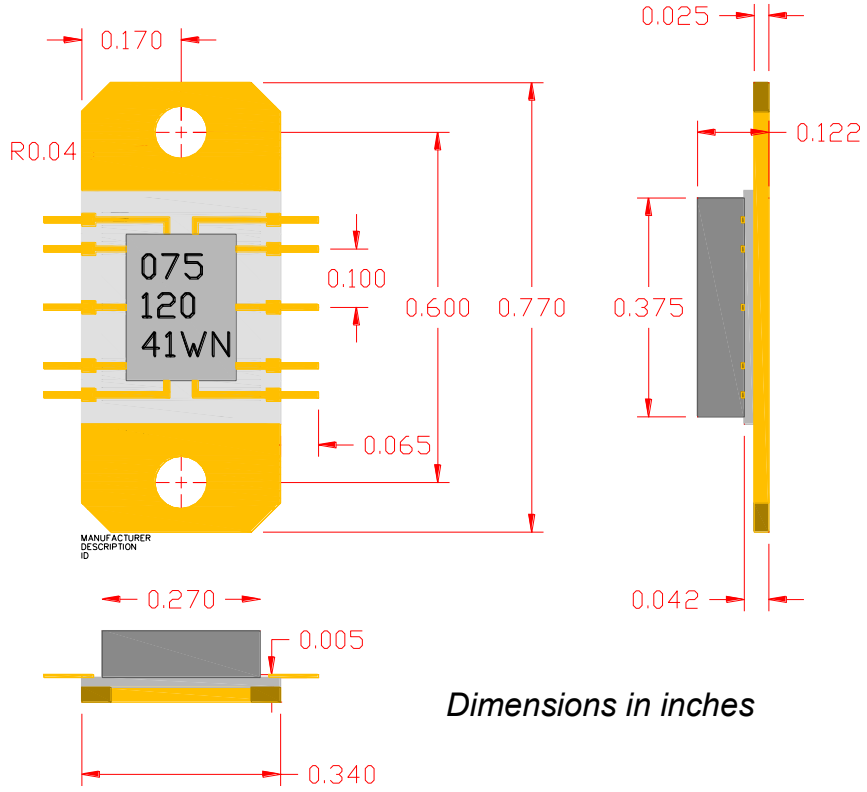
POWER DATA Vs VOLTAGE





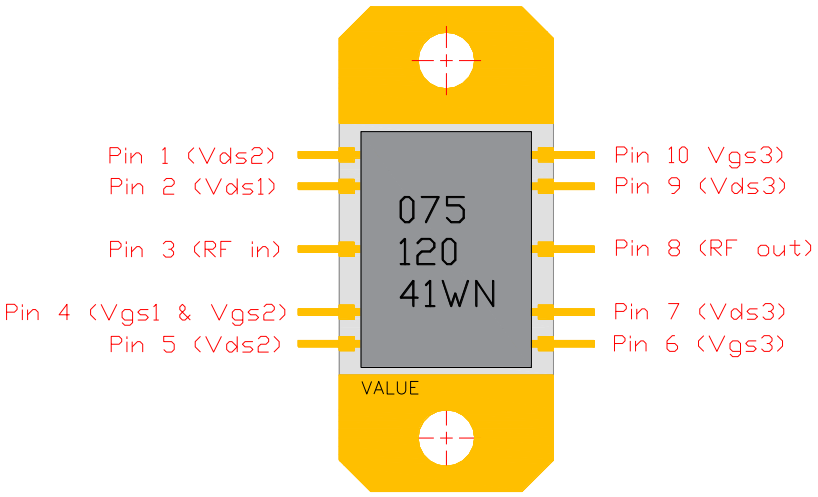
** Power measured using test fixture. Bias Conditions**: $V_{ds1,\,2,3}$ = +28V, $I_{dsq1+\,2}$ = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3} =-1.8V.

PACKAGE OUTLINE



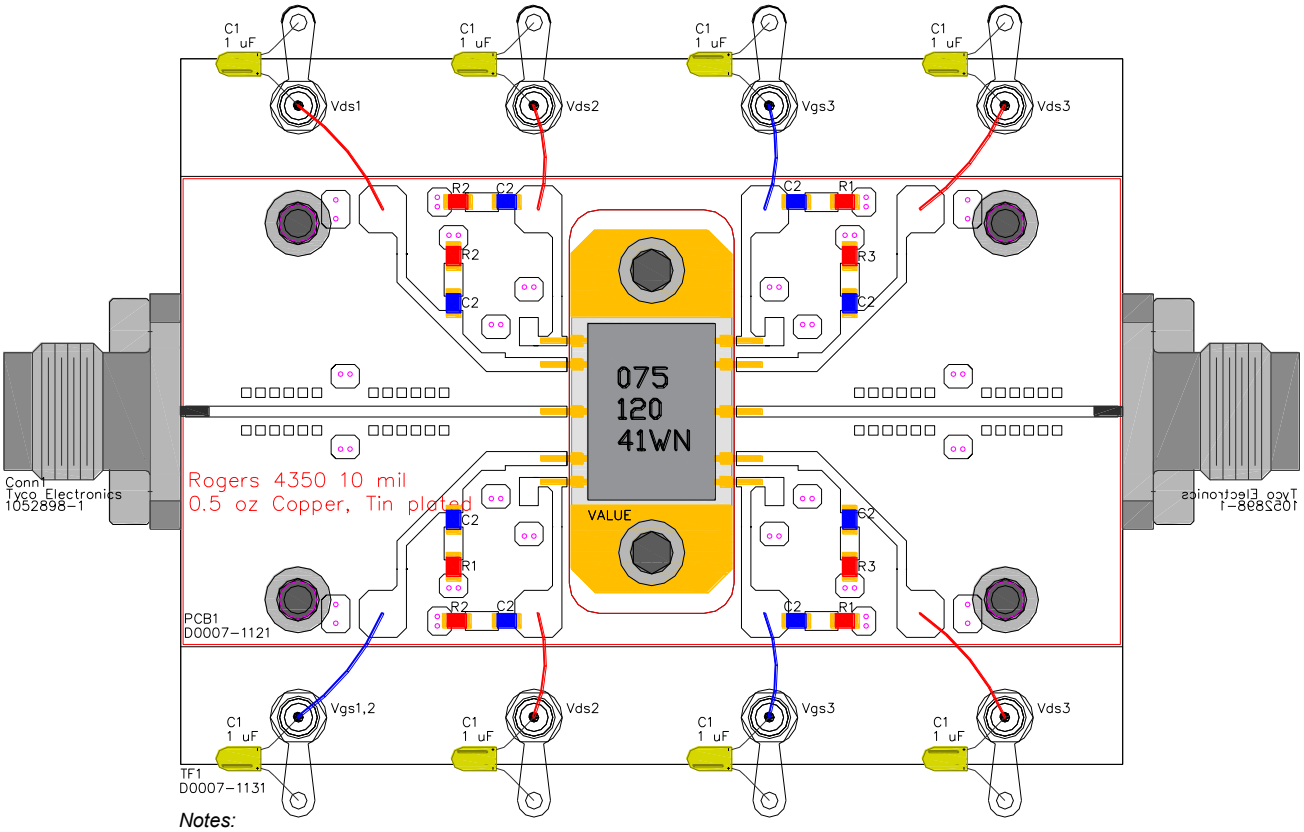
Dimensions in inches

Pin Layout



Pin No.	Function	Bias
1	Vds2	+28V
2	Vds1	+28V
3	RF in	-
4	Vgs1 & Vgs2	-1.8V
5	Vds2	+28V
6	Vgs3	-1.8V
7	Vds3	+28V
8	RF out	-
9	Vds3	+28V
10	Vgs3	-1.8V

TEST CIRCUIT



Notes:
1- Use epoxy to mount PCB
2- C1=1uF, C2=1000pF, R1=50ohms, R2=10ohms, R3=5ohms
3- All SMT Caps & Resistors are 0603 size
4- Use Test Block No. D0007-1131

Important Notes:

1- For best RF performance we recommend using 4mil indium shim between MMIC package and heatsink

2- Recommended current biases are 650mA for first and second stage combined and 900mA for the third stage. Gate biases of -1.8V are for reference only. Gate voltages could be adjusted to vary the currents going thru drain pins.

3- Do not apply drain voltages without proper negative voltages on gates. Otherwise MMIC would fail due to excess heat.

4- AutoCAD DXF available.