Product Brief	
Title	O3K 10Gbps Down Link (O3K10GDL)
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The **O3K10GDL** is an FPGA IP core implementing an optical on-off keying (**OOK**) modem for non-coherent optical communication in downlink (**space-to-Earth**) and inter-satellite link (**ISL**) applications.

The system is designed to provide robust operation in the presence of atmospheric turbulence and pointing jitter. The architecture is based on **CCSDS 142.0-B** recommendation and supports a nominal signaling rate of **10 Gbps**. In addition, the architecture has been designed to allow straightforward adaptation to related optical communication standards, including SDA and ESTOL implementations.

The IP core supports adaptive coding and modulation (**ACM**) through different frame headers and allows frame-by-frame reconfiguration. Link parameters are automatically recognized by the receiver, enabling seamless adaptation without dedicated synchronization procedures, data loss, or interruption of data transmission.

Another key feature of the O3K10GDL is its **one-bit quantization** approach at both transmitter and receiver. This significantly reduces implementation complexity and eliminates the need for high-speed DAC and ADC, enabling low-cost and power-efficient optical communication terminals.

Typical applications include:

- LEO satellite optical downlinks
- Inter-satellite links (ISL)
- Small satellite missions
- Optical communication demonstrators
- Research and development platforms
- Ground-to-space optical communication experiments

The O3K10GDL is designed for low-cost, low-complexity, and robust optical communication systems.

Figure 1 shows a simplified block diagram of the IP core.

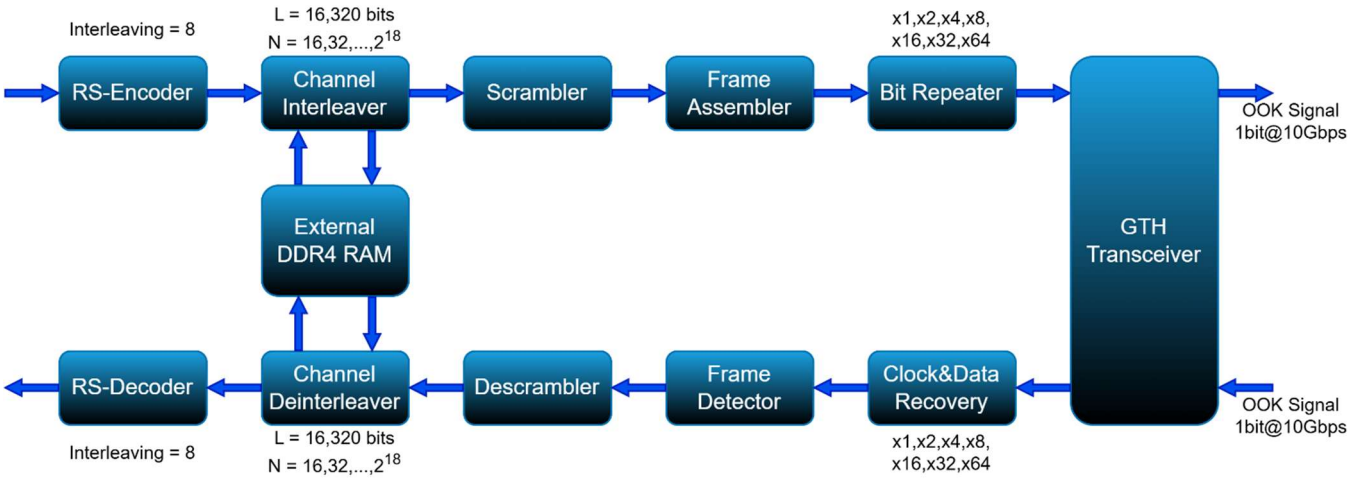

Figure 1: IP-core overview

Table 1 shows preliminary FPGA resource utilization estimates for a Xilinx UltraScale+ device.

Resource	Number
Look-Up-Tables (LUT)	110,000
Registers (FF)	87,000
Memory Blocks (BRAM)	69
Multiplier (DSP)	4

Table 1: Resources Consumption

Next table shows IP-core parameters.

Parameter	Min	Typ	Max
Supported applications	Downlink, ISL		
Modulation scheme	On-Off-Keying		
Adoptive coding and modulation (ACM) support	Yes		
Quantization Tx, Rx	1 bit		
Supported FPGA family	Xilinx UltraScale+		
RS-Code	[n=255, k=223], symbol width 8 bits		
RS-Code interleaving depth	fixed to 8		
Scrambling	Yes		
Attached synchronization marker (ASM) insertion	Yes		
Number of different ASMs (number of ACM configurations)	8		

Bit repetition factors	1x, 2x, 4x, 8x, 16x, 32x, 64x		
Number of bits in interleaving row	fixed to 16320		
Number of interleaving rows	16,..., 2^18 in steps of 16		
Sampling rate at transmitter, GHz		10	
Sampling rate at receiver, GHz		20	
User data rate, Gbps	0.14		8.75

Table 2: IP-Core Parameters

BellComTec offers support for feasibility studies, FPGA integration, custom developments, verification activities, and system-level optimization for optical communication applications.